CML Semiconductor Products

Obsolete Product
- For Information Only -

PRODUCT INFORMATION

PUBLICATION D/2030/1
MARCH 1983

Island Labs

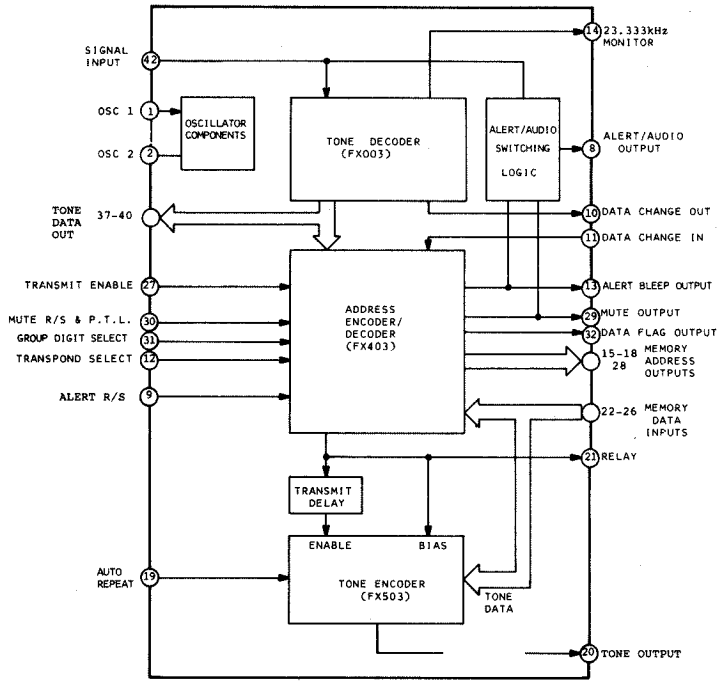


FIGURE 1 INTERNAL BLOCK DIAGRAM

FX2030C
FX2030Z
LOW POWER SELECTIVE CALLING ENCODER/ DECODER HYBRID

FEATURES

* LOW POWER CONSUMPTION
* SMALL PHYSICAL SIZE
* COMPLETE ENCODER/DECODER/TRANSPONDER
* CHOICE OF CCIR OR ZVEI TONE-SETS
* INCLUDES ALERT BLEEP GENERATOR
* INCLUDES GROUP CALL DECODING
* AUDIO SWITCHING
* FEW EXTERNAL COMPONENTS
* SIMPLE INTERFACING
* DATA DECODING

DESCRIPTION

The FX2030 is a complete selective calling encoder/ decoder for 5-tone sequential systems. It offers the advantages of small size, low power consumption, simple interfacing and high performance.

The thick film hybrid combines LSI CMOS chips with discrete resistors, capacitors and diodes to minimise the number of external components required. The FX2030C is based on the CCIR signalling frequencies and the FX2030Z is tuned to the ZVEI tone-set.

DECODER

A typical sequence of operation is illustrated in Figure 2. The FX2030 decodes a correct selective call and automatically transponds an acknowledgement in reply. The hybrid will then switch the Mute output high and generate an alert call to warn of an incoming message. Finally the incoming speech signals are switched through to the output.

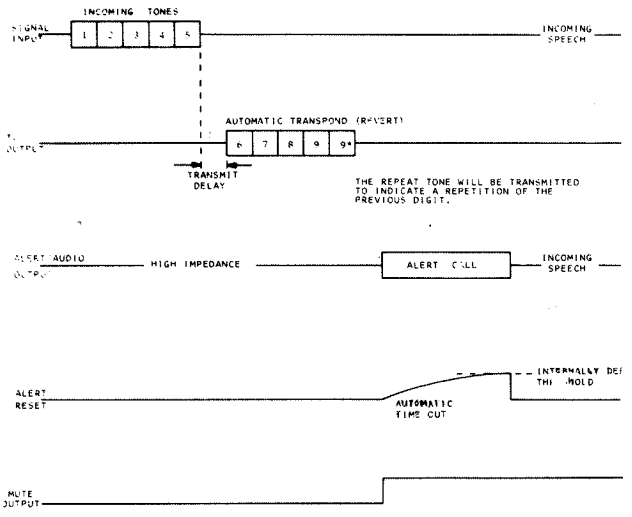


FIGURE 2 TYPICAL TRANSPONDER SEQUENCE

ENCODER

The encoder section of the FX2030 is enabled either in response to a transmit instruction (Tx) or for automatic transpond (Tp) as illustrated in Figure 2.

EXTERNAL COMPONENTS

To provide a selcall encoder/decoder function the FX2030 requires a few external components as shown in Figure 3.

560kHz Oscillator.

The receiver tone channels, encoder output frequencies and alert patterns together with system timing functions are derived from the 560kHz reference. A low cost ceramic resonator can be directly driven by the circuit together with a trimmer capacitor to adjust the frequency as shown. Pin wiring should be kept short.

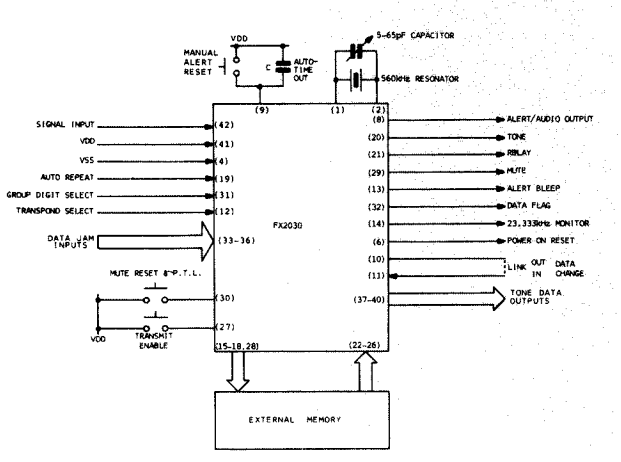


FIGURE 3 EXTERNAL COMPONENTS

The 560kHz can be measured by monitoring Pin 14 and adjusting the logic level square wave to 23.333kHz. Monitoring Pin 14 avoids directly loading the oscillator with a frequency counter. All necessary calibration is now complete.

For some applications the small frequency drifts associated with temperature and ageing effects may be unacceptable. In this case a crystal derived clock can be injected at Pin 2. Under no circumstances should power be applied to the device with no clock present. This would cause the dynamic logic to malfunction and could damage the device.

Alert Reset.

Adding a capacitor to the Alert Reset input (between pins 9 and 41) provides an automatic time out of alert signals. A N/O switch to VDD can be used for manual reset.

PIN DESIGNATIONS

Pin

1. Osc. 1
2. Osc. 2
3. Not connected
4. VSS (negative supply)
5. Not connected
6. Power on reset
7. Not connected
8. Alert/Audio output
9. Alert reset input
10. Data change output
11. Data change input
12. Transpond select input
13. Alert bleep logic output
14. 23.333kHz monitor output
15. AO memory address output
16. A1 memory address output
17. A2 memory address output
18. A4 memory address output
19. Auto repeat input
20. Tone output
21. Relay output
22. DpO(2) memory data input
23. DpO(1) memory data input
24. Dp1 memory data input
25. Dp2 memory data input
26. Dp3 memory data input
27. Transmit enable input
28. A3 memory address output
29. Mute output
30. Mute reset & P.T.L. input
31. Group digit select input
32. Data flag output
33. DjO data jam input
34. Dj1 data jam input
35. Dj2 data jam input
36. Dj3 data jam input
37. Q3 tone data output
38. Q2 tone data output
39. Q1 tone data output
40. Q0 tone data output
41. VDD (positive supply)
42. Signal input

TECHNICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

SUPPLY VOLTAGE ..... -0.3V to 7.0V
INPUT VOLTAGE AT ANY PIN (ref VSS = OV) ..... -0.3V to (VDD + 0.3)V
OUTPUT SINK/SOURCE CURRENT (TOTAL) 20mA
OPERATING TEMPERATURE RANGE ..... -20°C to +60°C
STORAGE TEMPERATURE RANGE ..... -40°C to +85°C
MAXIMUM DEVICE DISSIPATION 100mW

OPERATING LIMITS

Unless otherwise stated VDD = 5V, T_A = 25°C, ϕ = 560kHz, Gaussian White Noise (band limited to 6kHz), $\triangle$fo = o, Input Tone Period { 100ms per tone CCIR / 70ms for ZVEI

CHARACTERISTICS		MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS					
Supply Volts		4.5	5.0	5.5	V
Supply Current (In receive mode)			1.5		mA
Supply Current (In transmit mode)			3.5		mA
Input Impedance Pins 2, 12, 19, 27, 31, 33-36			1		MΩ
Input Impedance Pins 9, 30			2.2		MΩ
Input logic '1' } All logic inputs		3.5			V
Input logic '0' } All logic inputs				1.5	V
Logic '1' O/P Isource = 0.1mA } Pins 10, 14-18, 29,		4.0			V
Logic '0' O/P Isink = 0.1mA } 32, 37-40				1.0	V
Logic '1' O/P Isource = 0.3mA } Pin 28		4.0			V
Logic '0' O/P Isink = 0.8μA } Pin 28				1.0	V
Logic '1' O/P Isource = 0.05mA } Pin 13, 21		4.0			V
Logic '0' O/P Isink = 0.05mA } Pin 13, 21				1.0	V
Output source current Pin 6				300	nA
DYNAMIC CHARACTERISTICS					
DECODER					
Decode Input Sensitivity		40			mVrms
Decode Bandwidth P>0.995 any tone	FX2030C	±1			
at Signal/Noise ratio >3dB	FX2030Z	±2			%
Not Decode Bandwidth	FX2030C	±3			
(P<0.03 any tone)	FX2030Z	±4.5			%
Signal/Noise Ratio for P>0.97 (any 5 tone call sequence)		0			dB
ENCODER					
Tone output emf pin 20		120	160	185	mVrms
Tone output source impedance pin 20			1		kΩ
Tone duration	FX2030C	98	100	102	ms
	FX2030Z	68	70	72	ms
Tone encode accuracy ($\triangle$f)	FX2030C			±4	Hz
	FX2030Z			±0.3	%
Transmitter lead time (Tx Delay)		150	210	290	ms
AUDIO PATH					
Input Impedance (speech path switch open circuit) pin 42		1.75			MΩ
Speech path switch impedance (i.e. 'on') between pins 42 and 8			1		kΩ
Speech path switch isolation (i.e. 'off') between pins 42 to 8			50		dB
ALERT					
Alert call frequency			2.121		kHz
Alert output level (into 1kΩ) at pin 8			275		mVpk-pk
Alert output level (into 10k) at pin 13			2.0		Vpk-pk

	MIN	TYP	MAX	UNIT
Alert time out using external capacitor C in μF on pin 9	1.57C	2.1C	2.63C	s
Leakage current of capacitor C			0.7	μA
Recommended range of external capacitor C	0.33		4.7	μF
Internal pull-up resistor pin 9	2.09	2.2	2.31	MΩ
Switchover time from Alert to incoming speech at pin 8		0.6		s
TIMINGS				
Osc. 2 input pulse width (pin 2) (using external clock)	750	893	1000	ns
Power On Reset (pin 6) input pulse width	2			ms
Alert Reset (pin 9) input pulse width	10			μs
Data Change input (pin 11) pulse width	100			μs
Transmit Enable (pin 27) input pulse width	100			μs
Transmit Enable pulse rise time			10	μs
Mute Reset & P.T.L. (pin 30) input pulse width	90			μs

SIGNALLING FREQUENCIES (in Hertz)

Tone	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E
FX2030C	1981	1124	1197	1275	1358	1446	1540	1640	1747	1860	2400	930	2247	991	2110
FX2030Z	2400	1060	1160	1270	1400	1530	1670	1830	2000	2200	2800	810	970	886	2600

Table 2 shows the response of the FX2030 under various input conditions.

TABLE 2

TRANSMITTED TONES (Note 1)	TRANSPOND SELECT (Note 2)	TRANSPOND OUTPUT	ALERT OUTPUT (Note 3)	ALERT AUTO TIME OUT	AUDIO SWITCH (Note 4)	COMMENTS
12345	1	Yes	Address call	Yes	On	Address call. Transpond selected.
12345	0	No	Address call	No	Not applicable	Address call. No auto time-out. Transpond not selected.
1234A or AEAEA	X	No	Group call	Yes	On	Group call or all-call. Transpond automatically inhibited.
12345C	1	No	Address call	Yes	On	Address call. Reverses Transpond selection.
12345C	0	Yes	Address call	Yes	On	Address call. Reverses Transpond selection.
12345B6789	1	Yes	Second address/data	No	Not applicable	Addressed data (6789). No auto time out.
1234AB	X	No	Second address/data	No	Not applicable	Group call using second address. Transpond automatically inhibited.
12345D	1	Yes	None	Not applicable	Off	'silent interrogate'/mute and reset. Transpond if programmed.
AEAEAD	X	No	None	Not applicable	Off	Mute and reset all receivers. Transpond automatically inhibited.
12345CB	1	No	Second address/data	No	Not applicable	Second address call. Reverses transpond selection.
12345CD	1	No	None	Not applicable	Off	Individual mute & reset. Reverses transpond selection.
123456	X	No	None	Not applicable	Off	Incorrect address with too many digits.

Notes: 1) The address code is 12345, A is group tone, E is repeat tone, B, C and D are address suffix tones.

2) Indicates input logic state, X = don't care.

3) Refer to Fig. 5 for alert patterns and timings.

4) Defines condition of audio switch after transpond and alert sequences are completed. 'Not applicable' arises where alert does not automatically time out and must be manually reset.

DESIGN INFORMATION

Pin Descriptions

OSC. 1 - Output of a CMOS inverter. Can be used in conjunction with the Osc. 2 input to form the active element of a ceramic resonator circuit. Passive components are included on the hybrid to complete the oscillator circuit.

OSC. 2 - Input of a CMOS inverter. Alternatively a logic level 560kHz square wave can be injected at this pin with Osc. 1 left open circuit.

VSS - Negative supply input.

POWER ON RESET - provides a positive going pulse when power is applied to the hybrid. The pulse can be used to automatically initialise external circuits but must not be excessively loaded. The power supply must rise to 90% of its final value within 2ms to ensure adequate function. Alternatively an external logic '1' pulse from a low impedance source can be applied after the power supply has stabilised.

ALERT/AUDIO OUTPUT - linear output pin. The logic level alert patterns are output at this pin via an impedance of approximately 15k ohms. The transmission gate between the Signal input and Alert/Audio output is disabled when alert patterns are being generated.

When the hybrid is unmuted the analogue signals at the Signal input are available at the Alert/Audio output.

ALERT RESET INPUT - Includes internal pull-up resistor. The input has a schmitt trigger characteristic to permit the use of slow rising voltages for automatic time out applications. A discharge transistor normally holds the pin close to the negative supply and is disabled for auto time out. The alert pattern is reset when the input voltage exceeds the schmitt trigger upper limit (typically 0.66 VDD volts).

A switch connecting to the positive supply can be used for manual reset.

DATA CHANGE OUTPUT - CMOS logic output. A logic 1 pulse is output each time the tone decoder detects a change of tone. Normally connected to:

DATA CHANGE INPUT - logic input. A logic 1 input pulse causes the address decoder to compare the tone code with the data held in the external address PROM.

TRANSPOND SELECT INPUT - logic input with pull-up resistor. A logic 1 or open circuit will cause the FX2030 to automatically transpond a reply after a selective call is decoded, and a logic 0 will inhibit this feature. Address suffix tone C inverts this selection and group calls inhibit transponding.

ALERT BLEEP OUTPUT - CMOS logic output. The alert patterns are available at this pin from a source impedance of typically 5k ohms. In the quiescent state the output is at VSS.

23.333 kHz MONITOR OUTPUT - CMOS logic output. This pin outputs a square wave frequency of 23.333kHz when the input clock is 560kHz. Most applications require a calibration tolerance of ±0.1%.

A0, A1, A2, A4 MEMORY ADDRESS OUTPUTS - CMOS logic outputs used to address the external memory.

AUTO REPEAT INPUT - logic input with pull-up resistor.

An open circuit or logic 1 enables the encoder auto repeat circuitry. This detects when the repeat frequency is required in an encode sequence.

Repeater access applications may require a continuous tone of two or more tone period durations. This can be encoded by disabling the auto repeat feature with a logic 0. The memory address outputs increment as normal after each tone period.

TONE OUTPUT - linear output. The output is held at VSS in the quiescent state.

The a.c. tone output signals are generated about a mean d.c. level of typically 0.25 volts.

RELAY OUTPUT - logic output. This pin outputs a logic 1 during a transmit sequence via a typical impedance of 15k ohms.

DPO (2), DPO (1), DP1, DP2, DP3 MEMORY DATA INPUTS - logic inputs. The 4 bit selcall address codes are input to the hybrid by these pins. The least significant bits are fed separately to the tone encoder DPO (2) and address encoder chip DPO (1). This allows the encoder to be programmed to the repeat frequency (code E) if required without causing shut-down of the system.

TRANSMIT ENABLE INPUT - applying a logic 1 level pulse at this pin acts as a transmit enable request. The internal components couple a pulse through to the address encoder.

A3 MEMORY ADDRESS OUTPUT - gives a CMOS logic 1 output level when a transmit enable request is accepted. The quiescent state is a logic 0 established by a 1M ohm pull-down resistor.

MUTE OUTPUT - CMOS logic output. The mute output is set to logic 1 at the start of an alert output sequence following receipt of a selcall. It is also forced high when the Mute Reset and P.T.L. input is activated and resets on the falling edge of the input pulse. Reset of the Mute output results when suffix D is included in an incoming address sequence or when a second address/data alert is reset at the Alert Reset input.

MUTE RESET AND PUSH TO LISTEN INPUT - logic input with pull down resistor. A logic 1 at the input activates the Mute output (P.T.L. feature) and resets an alert output sequence. The negative going input edge resets the Mute output.

GROUP DIGIT SELECT INPUT - logic input with on-chip pull-down resistor. The address decoder is programmed to recognise tone A as the group digit by a logic 0 or open circuit at this pin. A logic 1 programmes tone 0 as the group tone.

DATA FLAG OUTPUT - CMOS logic output. When address suffix B is decoded the Data Flag outputs a logic 1 and resets back to a logic 0 at the end of the tone sequence.

Dj0, Dj1, Dj2, Dj3 DATA JAM INPUTS. These pins connect directly to the tone data inputs of the address decoder, and 1M ohm resistors feed from the outputs of the tone decoder. Normal operation of the device requires these pins to be open circuited. Should it be required, for example, to abort address decoding data code F can be forced on these pins from low impedance sources (max. 10k ohms). A pulse at the Data Change input strobes the data into the device.

Q0, Q1, Q2, Q3 TONE DATA OUTPUTS - CMOS logic outputs. The current state of the tone decoder is output as a 4 bit word.

VDD - positive supply input.

SIGNAL INPUT - analogue input. The selective calling and speech signals are input to the hybrid at this pin.

DECODER OPERATION

Figure 4 is a flow diagram for the FX2030 decoder.

The tone decoder in the hybrid detects all valid input tone sequences.

The decoder limits the input signal and processes it in an autocorrelator. The autocorrelator has the effect of enhancing the coherence of signalling tones while rejecting random noise. The periodic signal information is detected and passed to accurate digital divide/count circuits where fifteen tone bands are simultaneously scanned by the decoder. These are tuned to detect the tone digits 0 to 9, repeat tone, group tone and three instruction tones. The divide/count outputs are further processed to optimise the performance of the decoder.

The tone data is compared by the address decoder chip with the data stored in an external memory. If an incorrect sequence is detected the decoder aborts and remains in standby until the end of the tone sequence. The decoder includes circuitry to identify when the repeat frequency is expected in an address sequence. It automatically programmes repeat in place of the code digit held in the address memory.

Group Calling.

Completely flexible group call decoding is provided by the FX2030, without constraints on the calling structure. The examples show Tone A representing the group call frequency and E being a repeat of the previous tone digit:

Transmitted Tones	Units Called
1234A	12340-12349
12AEA	12000-12999
A2345	02345-92345
AEAEA	All units

If a group tone is included as part of a correct incoming sequence the decoder sets an internal latch. At the end of the sequence the state of the latch is inspected and transponder operation will be inhibited for group calls. This avoids the situation where multiple receivers are simultaneously keyed.

Alert.

An alert output will be generated next in the sequence. It is however inhibited for 'Silent Interrogate' (refer to Suffix Tones section) as shown by the 'NO' branch in the flow diagram of Figure 4.

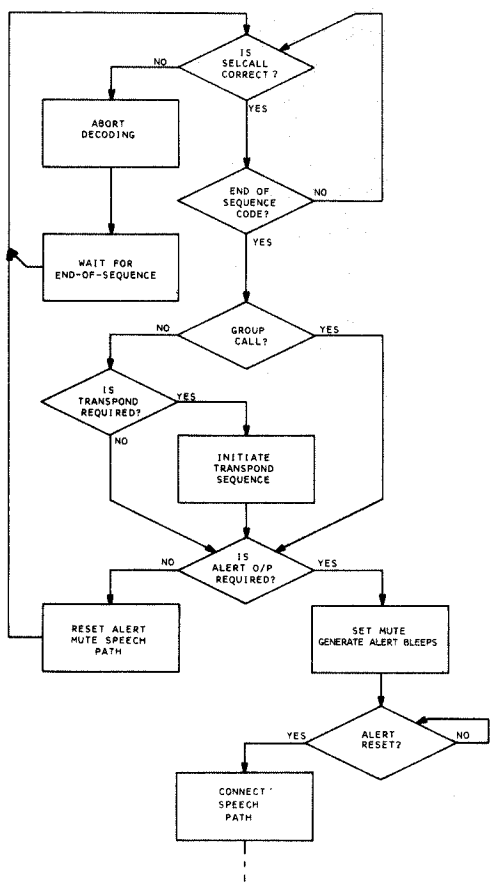


FIGURE 4 DECODER FLOW DIAGRAM

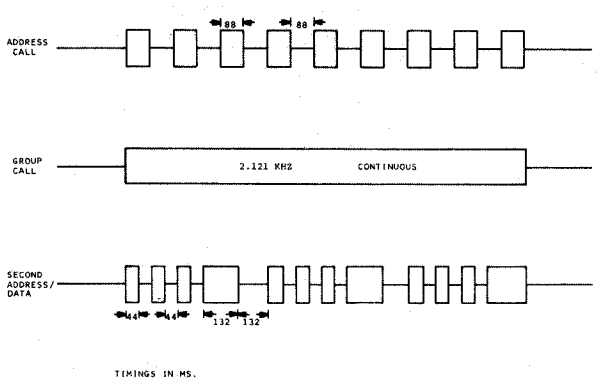


FIGURE 5 ALERT OUTPUT PATTERNS

The alert signal at the Alert/Audio output (Pin 8) is derived from the logic level square wave at Pin 13. The alert source impedance at Pin 8 is typically 15k ohms.

The 2.121kHz clock is chopped as shown in Figure 5. An even mark/space alert signals an address call and a continuous note indicates detection of a group call. A second address/data call is announced by the distinctive pattern shown.

The alert can be automatically reset by providing a capacitor 'C' on the Alert Reset input Pin 9. Automatic time out is not available for address calls where a transpond is not selected or for second address/data calls. These must be reset externally by a logic 1 pulse at Pin 9.

An alert will also be cleared by activating either the Mute Reset & P.T.L. or Transmit Enable inputs.

Audio Squelch

The FX2030 features an audio switch in the signal path. This transmission gate is controlled by the decoder and is automatically turned on after the alert has reset. The speech signals at the Signal input are now available at the Alert/Audio output.

Pin 30 is the Mute Reset & P.T.L. Input and as its name implies offers two functions. Manual defeat of the mute is provided with a high level at this pin. The 'Push to Listen' action is used to check channel occupancy.

The falling edge of the input pulse at Pin 30 is detected and used to mute the receiver.

The remote mute facility is discussed in the Suffix Tones section.

Figure 6 (i) gives the timing relationships between the Tone Data outputs and the Data Change output. The Data Change strobe causes the Memory Address outputs to increment and the critical Memory Data input timings are detailed.

Figure 6(ii) shows the timings of the Mute output, Alert Bleep Logic output and the Alert/Audio output following receipt of a correct selcall.

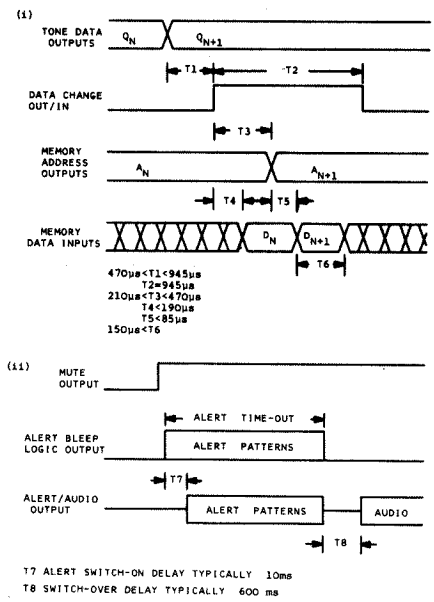


FIGURE 6 MEMORY AND ALERT OUTPUT TIMING RELATIONSHIPS

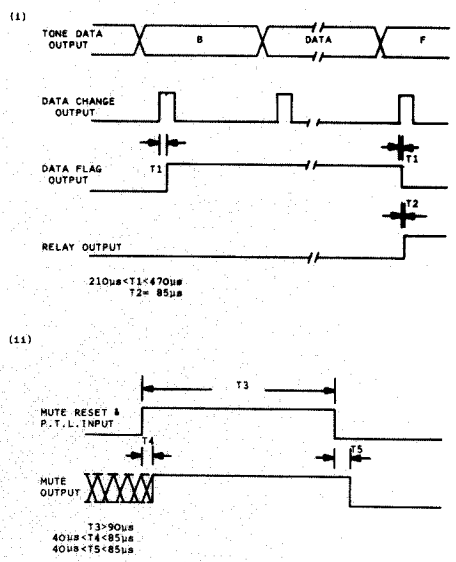


FIGURE 7 DATA AND MUTE OUTPUT TIMING RELATIONSHIPS

The Data Flag output relationships are detailed in Figure 7 (i) and the Mute and Mute Reset input in Figure 7 (ii).

ENCODER OPERATION

Transmit.

The hybrid can be used to transmit a code sequence as a calling or identity signal, as illustrated in the flow diagram of Figure 8.

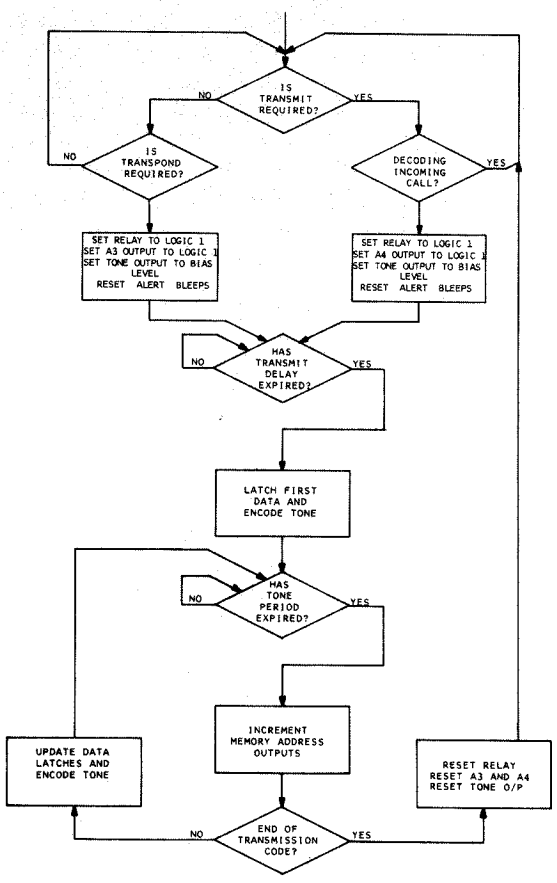


FIGURE 8 ENCODER FLOW DIAGRAM

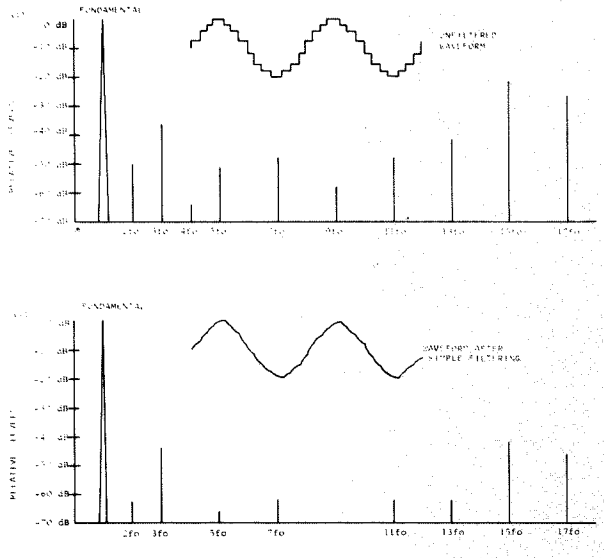


FIGURE 9 ENCODER OUTPUT WAVEFORM AND SPECTRAL ANALYSIS

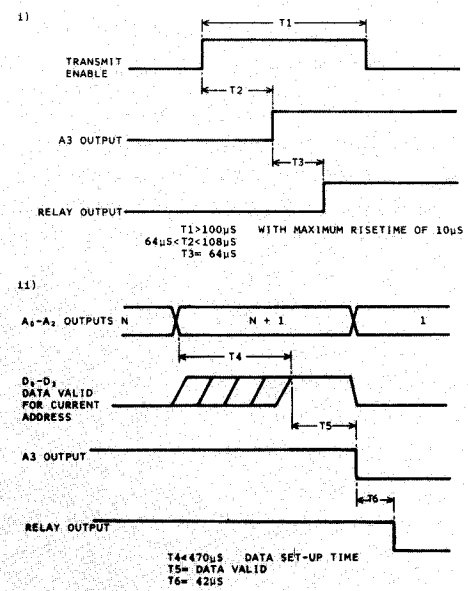


FIGURE 10 TRANSMIT ENABLE AND MEMORY TIMING RELATIONSHIPS

A positive pulse at the Transmit Enable input is coupled to the control chip (FX403) and will be accepted unless the decoder is processing an incoming selcall. The FX403 will enable the encoder chip (FX503) and set the Relay and A3 outputs high.

The Relay line is used to switch from the FX503 standby clock of 23.333kHz to a 560kHz clock used during encoding. This technique is used to reduce the overall power consumption to a minimum.

The Relay line is also used to start a delay period of typically 210ms. This transmit delay allows time to key the transmitter in a transceiver before the start of the first tone. Additionally the Tone output is set to a d.c. level of approximately 0.25 volts. The tones are generated about this mean d.c. level and the delay allows conditions to stabilise before encoding starts.

The tone data is read from the memory and automatically updated as required by the FX2030. Figure 9 (i) illustrates the tone waveform generated by the device together with the relative levels of the harmonics of the tone. The harmonic content can be further reduced if necessary by the simple filtering provided by a 0.1μF capacitor between the Tone output and VSS. This would yield the waveform and spectral response shown in Figure 9 (ii).

Each tone in the sequence is generated for an accurately timed period when the hybrid will automatically access the next memory location. The new data is inspected for the end of transmission instruction (code E) from the memory which causes the Relay and A3 outputs to be reset to logic 0. The Tone output will revert to its quiescent level (VSS) and the encoder chip is returned to the low current standby condition.

Transpond.

The transpond feature is used to automatically acknowledge correct decoding of a selective call. The reply signal can be decoded by the calling equipment to verify that contact is established.

The FX2030 is programmed into transpond mode by a logic 1 or an open circuit at the Transpond Select input (pin 12). Logic 0 on this pin will inhibit transponder operation. The encoder sequence is initiated immediately after the end of an incoming call as illustrated in Figure 2 and Figure 8. During the sequence both A4 and the Relay outputs will be at Logic 1 and will reset when the FX503 is disabled at the end of transmission. Figure 10 (i) gives the timing relationships between a pulse at the Transmit Enable input and the A3 and Relay outputs. In Figure 10 (ii) the outputs A_0-A_2 are shown addressing memory location N + 1. This contains code E which flags the end of an encode sequence.

SUFFIX TONES

The function of the FX2030 can be modified by adding extra tones after a selcall sequence. One or more of the three instruction tones B, C and D can be added to the end of a call.

Tone B.

Tone B can be used in a system in one of two ways.

Data messages can be added to selective calls by using additional tones to represent the data characters. Address and data sections of the call are separated by address suffix Tone B. The Data Flag output (pin 32) will be set high for data loading when tone B follows a valid address and remains high until the end of the tone sequence. The data is available as four bit words (hexadecimal) at the Tone Data Outputs (pins 37-40). Figure 14 shows the FX2030 interconnected to an FX313 display driver circuit.

The suffix Tone B also causes the circuit to generate a different second address/data alert output as illustrated in Figure 5. Automatic time-out of the alert is inhibited and can be reset by either the Transmit Enable or Mute Reset & P.T.L. inputs. If a selective call is transmitted with Tone B suffix but no data it can be used as a 'second address' facility.

A second address call could be used when a positive response such as 'contact the base' is required.

Tone B can be used in conjunction with C or D but must always be transmitted last in the sequence.

Tone C.

A call followed by Tone C will reverse the transpond selection programmed at Pin 12. Therefore a response can be inhibited from an equipment which normally replies or alternatively it can be requested. This feature may be employed in a system where not all equipments have the capability of decoding transponded calls. Including Tone C at the end of a transpond sequence will prevent the possibilty of transponder lock-up. This can occur where a transponded call is decoded and itself causes a further transpond.

Suffix Tone C is redundant for group calls.

Tone D.

Suffix instruction Tone D can be added to a call and results in two actions. Firstly it will both reset any alert running when the call was received, and inhibit an alert output. It will also mute the receiver audio by disabling the audio switch and reset the Mute output.

The mute and reset instruction does not affect the transponder operation of an address call so it forms a 'silent interrogate' instruction. Equally the suffix tone can be applied to an all-call to reset all the receivers on a system.

MEMORY CODING

The external memory contains the address code for the receiver, together with the transmit and transpond codes. The address digits are held as four bit (hexa-decimal) codes in the memory. Six different outputs from the hybrid could be used as address lines to the memory.

A0, A1 and A2 outputs increment in a binary count from 001 as shown below. These are used as the three least significant digits of the memory address. The A3 output goes high only for the time that a transmit instruction (from the P.T.T. button) is being encoded. Similarly A4 is set to logic 1 during a transpond sequence, while the Relay output is high whenever the hybrid is transmitting.

The interconnection chosen from the five options shown in Figure 11 will be governed by the requirements of the system.

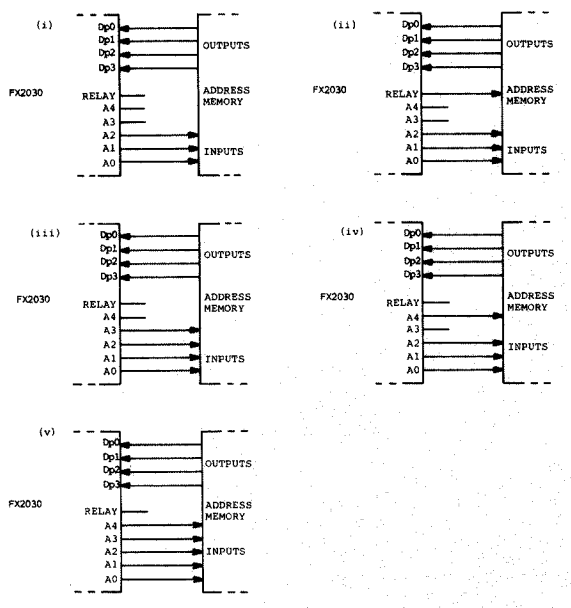


FIGURE 11 MEMORY INTERCONNECTION OPTIONS

The FX2030 fulfills the requirements of 5 tone selcall systems but is also compatible with other sequence lengths. The hybrid is instructed when the sequence is complete by code E in the memory as indicated. Therefore if for example four tones are required the fifth location would be programmed with code E as shown in example (v). Codes where two successive digits are the same do not require special programming. As illustrated in (ii) 67899 is coded as normal but the hybrid substitutes the repeat tone where necessary.

Illustration (i) is the simplest interconnection pattern. The outputs A0, A1 and A2 will provide indentical receive (Rx), transmit (Tx) and transpond (Tp) codes. An example of the codes held in the memory to give a call number 12345 would be:

Example (i) Rx code 12345
Tx code 12345
Tp code 12345

Memory location (binary)	001	010	011	100	101	110
Rx/Tx/Tp code (hexadecimal)	1	2	3	4	5	E

In (ii) the Relay output is used as an input to the memory. To programme 12345 as the receive code and 67899 for a calling number, the memory would contain:

Example (ii) Rx code 12345
Tx code 67899
Tp code 67899

Memory location (bin)	0001	0010	0011	0100	0101	0110
Rx code (hex)	1	2	3	4	5	E
Memory location (bin)	1001	1010	1011	1100	1101	1110
Tx/Tp (hex)	6	7	8	9	9	E

The interconnection pattern in (iii) utilises A3 output. It is used where the receiver code 12345 is automatically transponded but a different number 67899 is needed when the Transmit Enable button is pressed.

Example (iii) Rx code 12345
Tx code 67899
Tp code 12345

Memory location (bin)	0001	0010	0011	0100	0101	0110
Rx/Tp code (hex)	1	2	3	4	5	E
Memory location (bin)	1001	1010	1011	1100	1101	1110
Tx code (hex)	6	7	8	9	9	E

(iv) Should it be required to transmit (using Transmit Enable) the receive code as an identity, but an alternative code when transponding then interconnection (iv) is used.

Example (iv) Rx code 12345
Tx code 12345
Tp code 67899

Memory location (bin)	0001	0010	0011	0100	0101	0110
Rx/Tx code (hex)	1	2	3	4	5	E
Memory location (bin)	1001	1010	1011	1100	1101	1110
Tp code (hex)	6	7	8	9	9	E

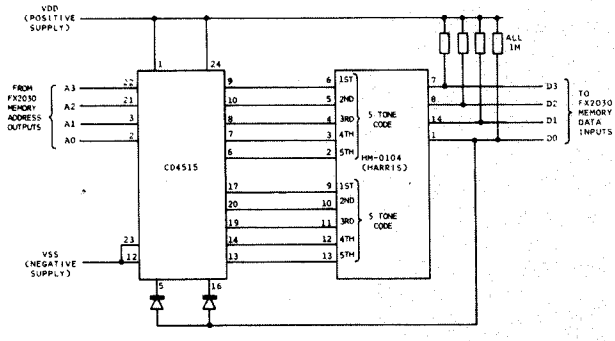


FIGURE 12 LOW POWER MEMORY

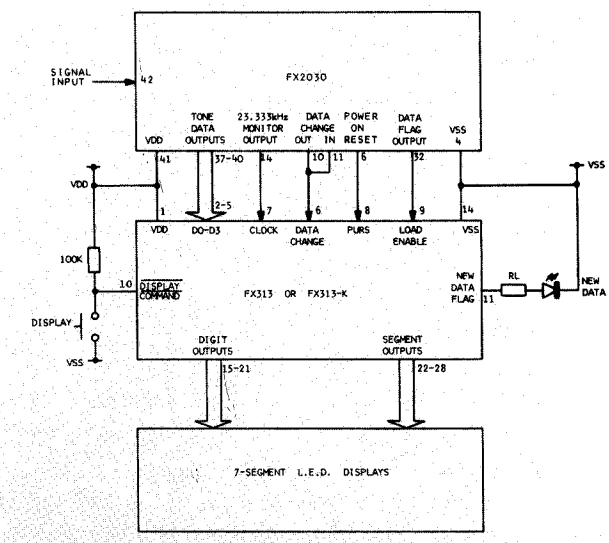


FIGURE 14 ADDITIONAL CIRCUITRY TO ADD LED DISPLAY DRIVER

(v) Connecting the FX2030 to the memory as (v) will give independent codes for receive, transmit and transpond. The five lines A0 to A4 are used to address the memory. Four tone sequential codes are illustrated.

Example (v) Rx code 1234
Tx code 6789
Tp code 4567

Memory location (bin)	00001	00010	00011	00100	00101
Rx code (hex)	1	2	3	4	E
Memory location (bin)	01001	01010	01011	01100	01101
Tx code (hex)	6	7	8	9	E
Memory location (bin)	10001	10010	10011	10100	10101
Tp code (hex)	4	5	6	7	E

Suitable memory types are fusible link PROM's or U.V. EPROM's in CMOS technology.

Applications requiring minimum possible power consumption can utilise a fusible link diode matrix and a 4-16 line decoder where space allows. The arrangement shown in Figure 12 has two independent five tone codes programmed into the matrix.

APPLICATIONS

The FX2030 is designed to provide selcall encode/decode facilities in application where both space and power consumption are prime considerations. Battery powered equipments such as hand-held radios provide an obvious example. Figure 13 shows the application of the FX2030 in a transceiver. The output from the demodulator is fed to the selcall signal input and the Alert/Audio output is connected to the audio amplifier. The Mute output can be used as an enable control.

A summing amplifier combines the microphone signals with the FX2030 Tone output before passing to the modulator. The transmitter section and aerial switching can be controlled by the Relay output combined with the P.T.T. button.

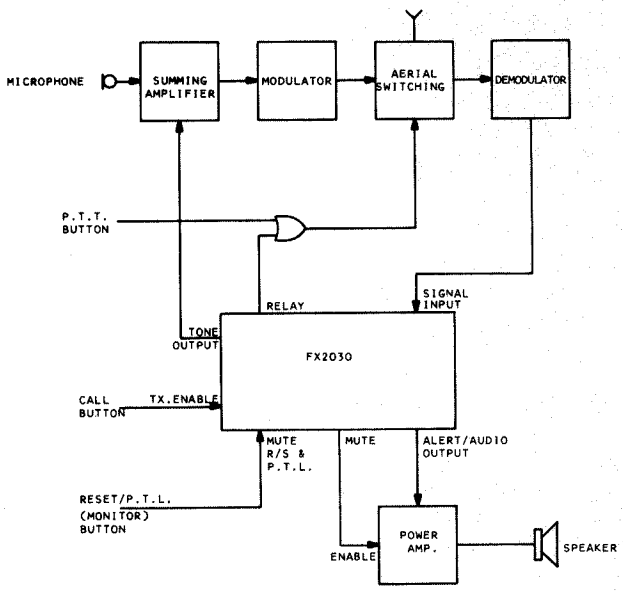
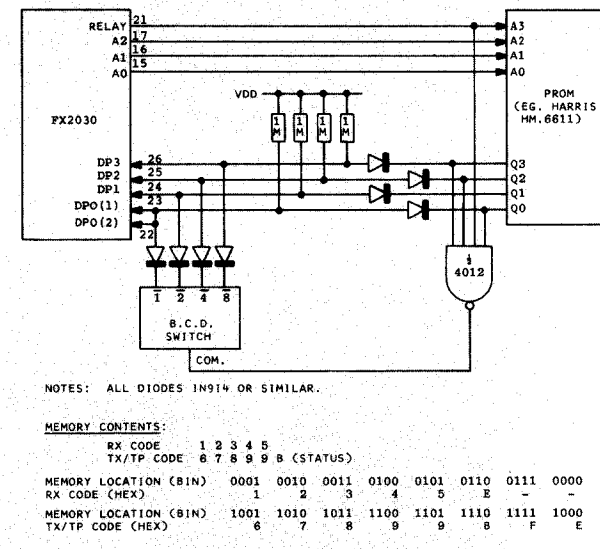


FIGURE 13 APPLICATION IN A RADIO TRANSCEIVER



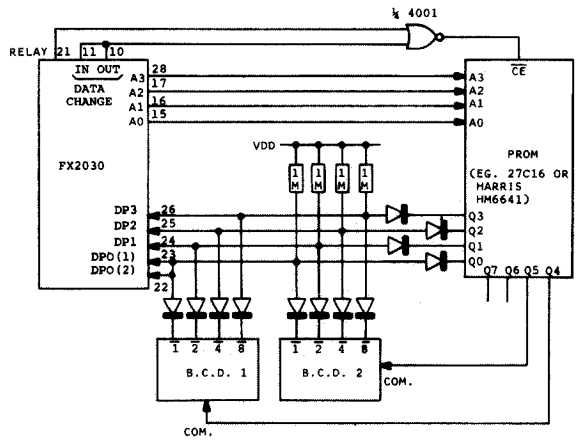
NOTES: ALL DIODES IN914 OR SIMILAR.

MEMORY CONTENTS:

RX CODE 1 2 3 4 5
TX/TP CODE 6 7 8 9 9 B (STATUS)

MEMORY LOCATION (BIN)	0001	0010	0011	0100	0101	0110	0111	0000
RX CODE (HEX)	1	2	3	4	5	E	-	-
MEMORY LOCATION (BIN)	1001	1010	1011	1100	1101	1110	1111	1000
TX/TP CODE (HEX)	6	7	8	9	9	B	F	E

FIGURE 15 ENCODING A SINGLE STATUS DIGIT



ALL DIODE IN914 OR SIMILAR.

MEMORY CONTENTS. SHOWN AS TWO HEXADECIMAL CHARACTERS.

RX CODE 1 2 3 4 5
TX/TP CODE 1 2 3 (SWITCH 1) (SWITCH 2)

MEMORY LOCATION (BIN)	0001	0010	0011	0100	0101	0110
RX CODE	F1	F2	F3	F4	F5	FE
MEMORY LOCATION (BIN)	1001	1010	1011	1100	1101	1110
TX/TP CODE	F1	F2	F3	EF	DF	FE

FIGURE 16 APPLICATION TO PROVIDE TWO VARIABLE TRANSMIT DIGITS

Figure 14 identifies the interconnection required to add an FX313 display/driver to a system. The LED displays data characters transmitted selectively to the hybrid.

The circuit shown in Figure 15 details the changes necessary to provide encoding of a single status digit. A high level at the FX2030 data input will be due to the effect of the pull-up resistor, while a low level is derived from forward biasing the diode.

The memory in this example has a 4-bit output, and must give a valid logic level at the FX2030 data input when the forward volt drop of the diode is included. The gate decodes the state during transmit when the memory data is F and enables the status switch. The DpO-Dp3 data inputs will then be coded via the diodes from the switch. The memory is programmed to decode 12345 as an address call number but to encode in either transmit or transpond a sequence 67899B followed by the status digit. Tone B is used in this instance to separate the 5-tone code from the status information tone to avoid aliasing selcall codes.

Figure 16 shows an efficient technique of enabling selector switches during a transmit sequence. The PROM is organised as an 8-bit output with 4 bits used to carry the hexadecimal tone codes. The 'common' input of each switch is allocated to one of the remaining memory outputs and is pulled low at the correct time by programming logic 0 at that output. These are shown as the hexadecimal codes E and D programmed into the Tx/Tp code sequence.

The circuit schematic shown is used to vary the last two digits of a 5 tone code. All receivers on the network would have the same first three digits, in this case 123XX. Up to 100 receivers could therefore be directly called using two selector switches.

The NOR gate shown in Figure 16 illustrates a technique for saving power. The FX2030 only requires to inspect the PROM data during decoding or encoding. The power dissipated at other times can be greatly reduced by disabling the memory. The chip enable or select input is therefore controlled by combining the Relay output with the Data Change output from the FX2030. The hybrid must always have logic levels applied at its inputs and these are provided by the pull-up resistors during standby.

INTERFACING AND ELECTRO-MAGNETIC COMPATIBILITY

The FX2030 requires a clock of 560kHz which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 560kHz or to its harmonics. Similarly the performance of the device could be impaired if high levels of radiated power were present near the high impedance offered by the Signal input.

During the time that the audio is muted the transmission gate between the input and output is disabled (pins 42 and 8). The impedance offered at the output is therefore very high. When the mute is lifted the hybrid closes the speech path with an impedance of typically 1k ohm. The changes in the loading effects on circuitry and any possible interference pick up from high impedances should be considered when interfacing the FX2030 into a system.

HANDLING PRECAUTIONS

The FX2030 contains CMOS LSI circuits which include input protection circuitry. However, precautions should be taken to prevent static discharges which can cause damage.

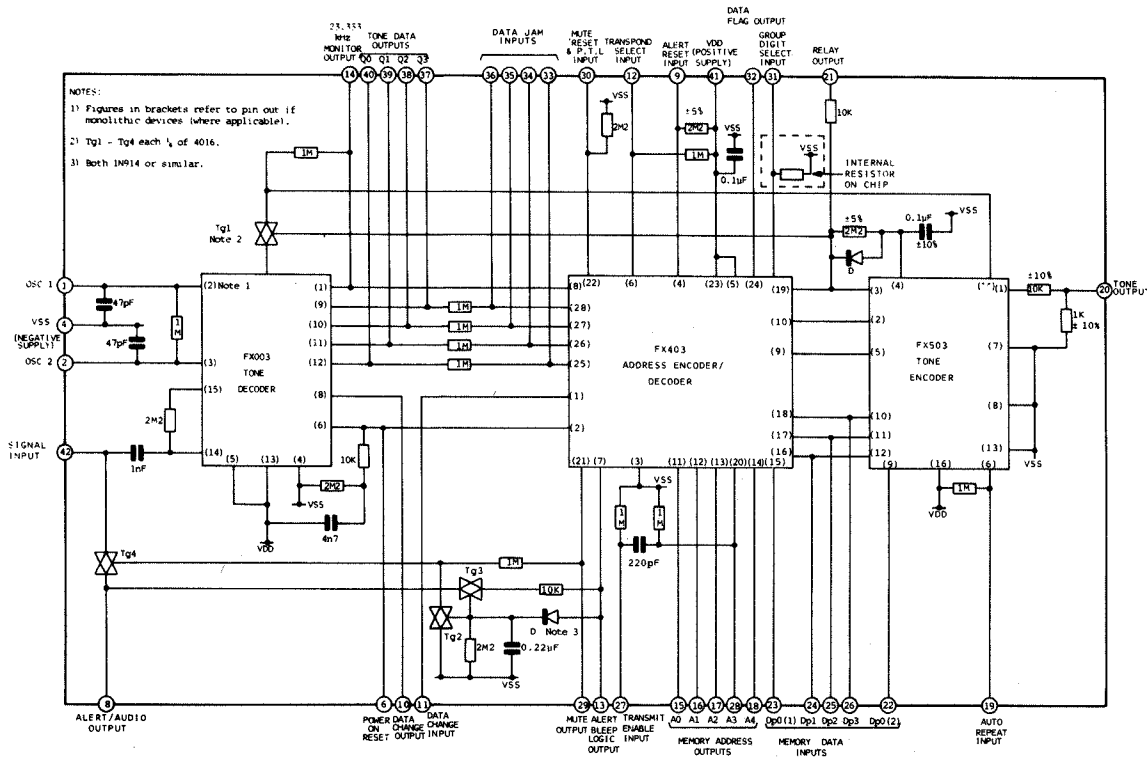


FIGURE 17 INTERNAL SCHEMATIC

MECHANICAL

The hybrid is constructed on ceramic substrates with the chips and other discrete components added. The chips are individually protected and the whole assembly is then coated to provide both mechanical and environmental protection. The package outline is given in Figure 18.

Pin 1 is identified on the package outline of Figure 18 and a '1' is printed on the top of the product.

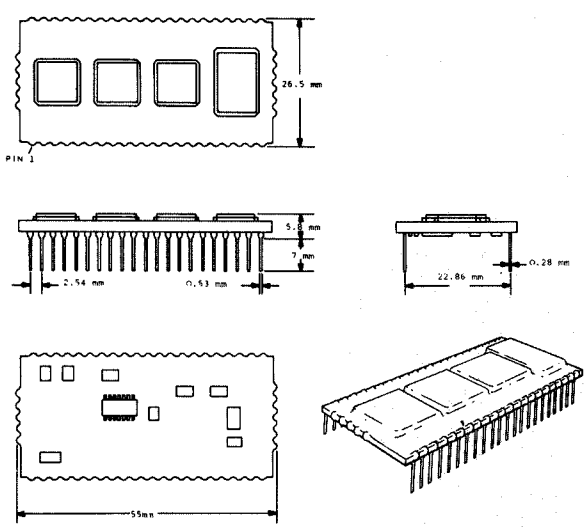


FIGURE 18 PACKAGE OUTLINE

NOTE:
CML does not assume any reponsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change said circuitry.