CONSUMER MICROCIRCUITS LTD

PRODUCT INFORMATION

Obsolete Product
- For Information Only -

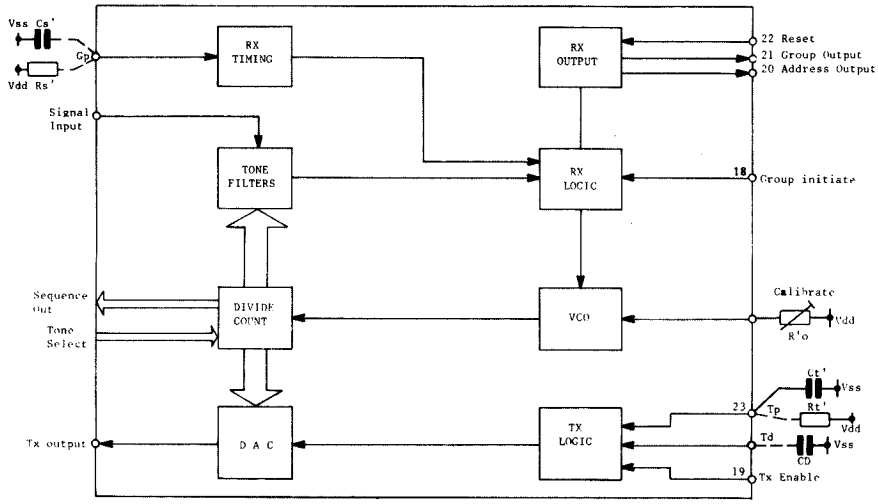
FUNCTIONAL SCHEMATIC

Island Labs

PUBLICATION D/4071/2/280

FX4070A
FX5070A
FX4071A
FX5071A

HYBRID INTEGRATED 5 TONE ENCODER/ DECODERS



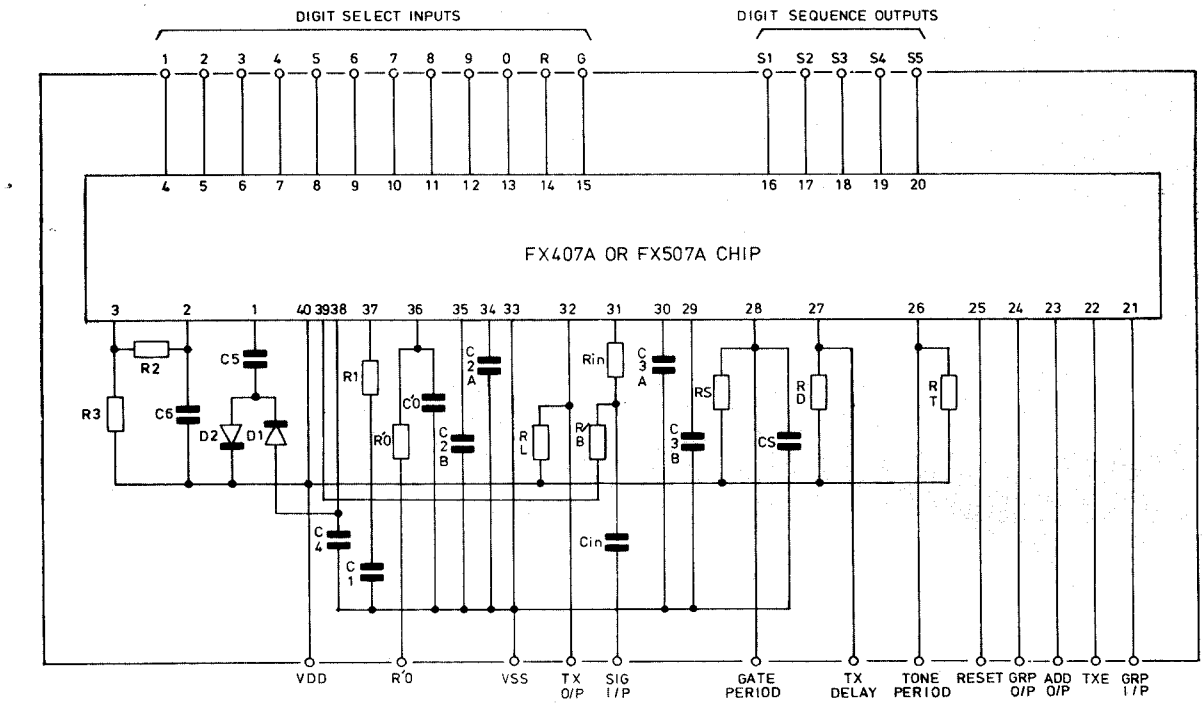
FEATURES

- FULLY FUNCTIONAL 5-TONE SELECTIVE CALLING SYSTEM
- THICK FILM HYBRID CONSTRUCTION
- USES CML FX407A/FX507A CHIP
- FIXED OR VARIABLE SYSTEM TIMING
- ENCODER, DECODER AND TRANSPONDER
- CHOICE OF PACKAGE STYLE

The FX 4070A, FX 5070A, FX 4071A and FX 5071A are integrated circuits fabricated using thick film hybrid techniques and include a monolithic LSI semiconductor chip. The circuit comprises all necessary components to provide a 5-tone selective calling encoder/decoder which complies with the requirements of the CCIR standard (FX 4070A or FX 4071A) or the ZVEI standard (FX 5070A or FX 5071A). In all respects the operation of these devices is identical to the recommended circuit used in the application of the CML FX 407A/FX 507A integrated circuit. The hybrid circuits include passive components necessary for correct system operation, the trimmer potentiometer required to set frequency calibration is externally connected and external components may also be used to modify internally set system timing parameters.

CIRCUIT DIAGRAM

INTERNAL CIRCUIT DIAGRAM OF HYBRIDS



HYBRID COMPONENT LIST (This information can be read in conjunction with Production Information on FX 407A)

RESISTORS

CIRCUIT DIAGRAM REF.	VALUE	TOLERANCE
R1	100K	5%
R2	100K	5%
R3	22K	5%
R'O	100K	5%
R'in	330K	10%
RD	680K	10%
RS(FX4070A/FX4071A)	1.22M	2%
RS(FX5070A/FX5071A)	857K	2%
RT	355K	2%
RL	600Ω	10%
R'b	330K	10%

CAPACITORS

CIRCUIT DIAGRAM REF.	VALUE	TC	TOLERANCE
C1	0.022μf	X7R	10%
C2A=C2B	470pf	X7R	10%
C3A=C3B	0.01μf	X7R	10%
C4	0.22μf	X7R	10%
C5	0.01μf	X7R	20%
C6	68pf	NPO	5%
C'O	0.01μf	NPO	5%
C'in	0.01μf	X7R	20%
Cs	0.22μf	X7R	20%

CALIBRATION PROCEDURE

Conditions: VDD = 12.5V, TA = 20° ± 5°, no input signals.

1) Programme code 6XXXX(FX4070A/FX4071A) or 5XXXX(FX5070A/FX5071A), where 'X' is any convenient digit.
2) Apply VDD. Wait several seconds, then connect a shorting link between pins 23 and VSS.
3) Press the TX Enable button and read the frequency at the TX output. The signal is a continuous tone.
4) Adjust the R'o calibration potentiometer until the frequency is exactly 1541Hz (FX4070A/FX4071A) or 1530Hz (FX5070A/FX5071A).
5) Remove the shorting link between pins 23 and VSS. Calibration is now completed for all channels for both RX and TX.

EXTERNAL COMPONENT CONNECTIONS

1. The address and group outputs are open drain MOS transistors. This allows the outputs to be linked to give a wire – OR if required. Load resistors (10KΩ nom.) are required for these outputs from pin 20 and pin 21 to -Ve supply.

2. A 22KΩ trimmer potentiometer with a temperature coefficient <100ppm must be connected from R'O to -Ve supply (pin 32). This is used to calibrate frequency as described above.

3. The Output Reset input has an on-chip 1MΩ (nominal) resistor to VDD and a 3KΩ M.O.S. transistor to VSS which is disabled when the outputs are activated. With this input held at VSS the outputs will turn on at power-up. To reset the outputs and to ensure they are off at power-up the pin must be momentarily taken to VDD. An automatic time-out commencing from when the outputs are activated is provided with a resistor in parallel with a capacitor between pins 22 and 32. The interval T'on ≏0.65 RC seconds, and should be longer than one tone period.

4. A capacitor (CT) must be provided between pin 23 and the positive supply (VSS) to set the transmitted tone period.

   The period is given by:

   $$Tp = 0.355K\ CT \text{ seconds.}$$

   where CT is measured in μF

   K = 0.6 ± 0.03 typ. (a constant of the monolithic chip)

   For CCIR tone period = 100 mS (FX4070A or FX4071A) then CT = 0.47μF
   For ZVEI tone period = 70 mS (FX5070A or FX5071A) then CT = 0.33μF

5. Optionally:

   i) A capacitor (CD) can be connected between the TX Delay pin and the positive supply (VSS) to provide a delay prior to the start of transmission.

   TX delay period = 0.68K CD seconds *

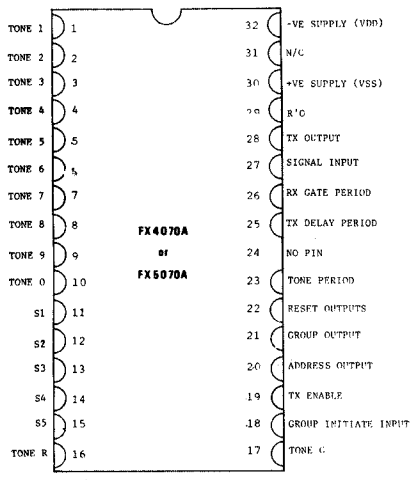
   ii) The RX gate period (internally set to 1.75 Tp) can be varied by external components connected in parallel to RS and CS.

   RX gate period = K RS' CS' seconds *

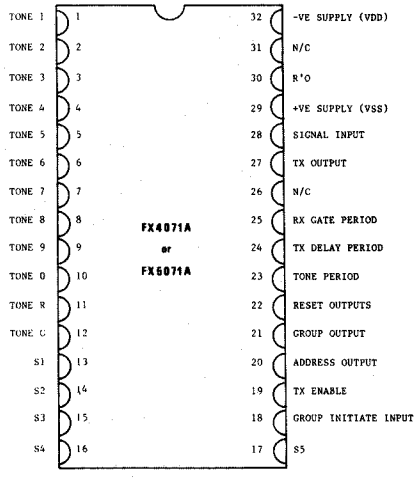
   * where K = 0.65 ± 0.033 typ. RS' and CS' are resultant values of internal and external components, CD and CS' are measured in μF
   RS' is measured in Megohms

PACKAGE DETAILS

FX4070A/FX5070A PIN CONFIGURATION



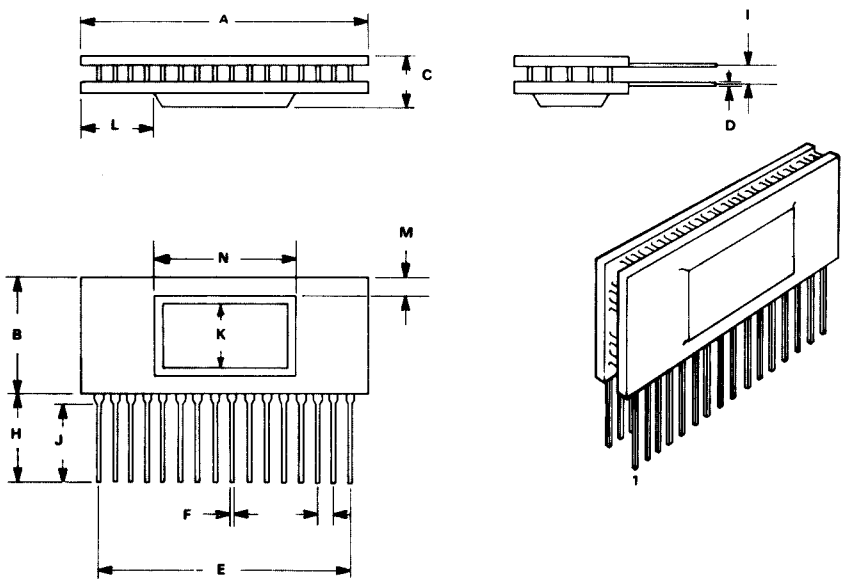
FX4071A/FX5071A PIN CONFIGURATION



FX 4070A and FX 5070A PACKAGE

	Inches	m.m.
A	1.675	42
B	0.675	17
C	0.35	8.9
D	0.01	0.25
E	1.5	38.1
F	0.02	0.51
G	0.1	2.5
H	0.425	10.8
I	0.1	2.54
J	0.4	10.0
K	0.4	10.0
L	0.4	10.0
M	0.085	2.16
N	0.9	22.9

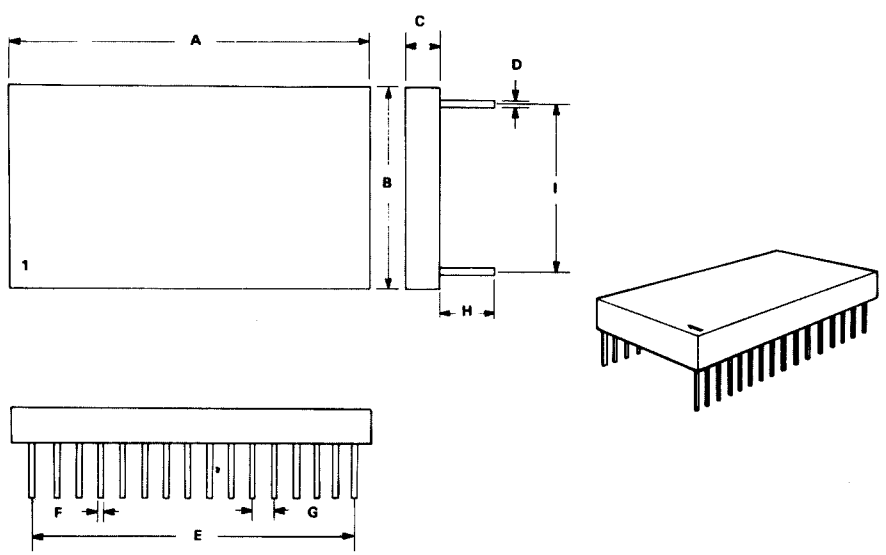
WORKING TEMPERATURE RANGE: -20°C to + 80°C
STORAGE TEMPERATURE RANGE: -40°C to + 85°C



FX 4071A and FX 5071A PACKAGE

	Inches	m.m.
A	1.77	45
B	1.18	30
C	0.2	5.1
D	0.01	0.25
E	1.5	38.1
F	0.02	0.51
G	0.1	2.54
H	0.325	8.26
I	0.9	22.9

WORKING TEMPERATURE RANGE: -20°C to + 80°C
STORAGE TEMPERATURE RANGE: -40°C to + 85°C



ELECTRICAL CHARACTERISTICS

	MIN.	TYP.	MAX.	NOTE
Supply voltage	-10V		-15V	
Supply current		15mA		
Operating Temperature	-20°C		+60°C	

ELECTRICAL CHARACTERISTICS AT VDD = 12 volts & T'amb = 20°C unless otherwise specified.

Input voltage logic '1'	-8.0V			Note 1.
Input voltage logic '0'			-1.5V	
Output voltage logic '1'	-10.0V			Note 2.
Output voltage logic '0'			-1.0V	

OPERATING FREQUENCIES (fo of bandpass filters and Tx O/P) see Calibration Procedure.

Digit 1		1121Hz	1057.5Hz		
2		1200.5Hz	1163Hz		
3		1278Hz	1269Hz		
4		1357Hz	1402Hz		
5		1444Hz	1530Hz		
6	FX4070A	1541Hz	1665.5Hz	FX5070A	
7	FX4071A	1638Hz	1828Hz	FX5071A	
8		1747Hz	2001Hz		
9		1856.3Hz	2203Hz		
0		1983Hz	2403Hz		
R		2113Hz	2601Hz		
G		2401Hz	2796Hz		
Frequency stability Δf/°C				0.015%	Temperature range -20° +60°C
Frequency stability Δf/Vsupply				0.015%	Supply voltage range -10 to -15V

DECODER OPERATION

Sensitivity		50mV		r.m.s
Max. Signal Handling	700mV			r.m.s.
100% decode BW	3%			FX4070A & FX4071A
	4%			FX5070A & FX5071A referred to fo
0% decode BW			6%	FX4070A & FX4071A
			9%	FX5070A & FX5071A referred to fo
Input impedance		100KΩ		

ENCODER OPERATION

Output voltage	1V			peak to peak output
Tone period	90mS	100mS	110mS	FX4070A & FX4071A with recommended value of CT
	63mS	70mS	77mS	FX5070A & FX5071A
Output impedance		600Ω		

Note 1. Pins 1-10, 16-19, 22 FX4070A & FX5070A
Pins 1-12, 18, 19, 22 FX4071A & FX5071A

2. RLOAD=10KΩ Pins 11-15, 20, 21 FX4070A & FX5070A
RLOAD=10KΩ Pins 13-17, 20, 21 FX4071A & FX5071A

CODE PROGRAMMING

Programming is achieved by links between the sequence outputs and the digit select inputs. The repeat code (R) is substituted for consecutive identical digits, e.g. 39999 is coded 39R9R. Should the fifth digit be common to any other digit it must be linked via a diode as shown.

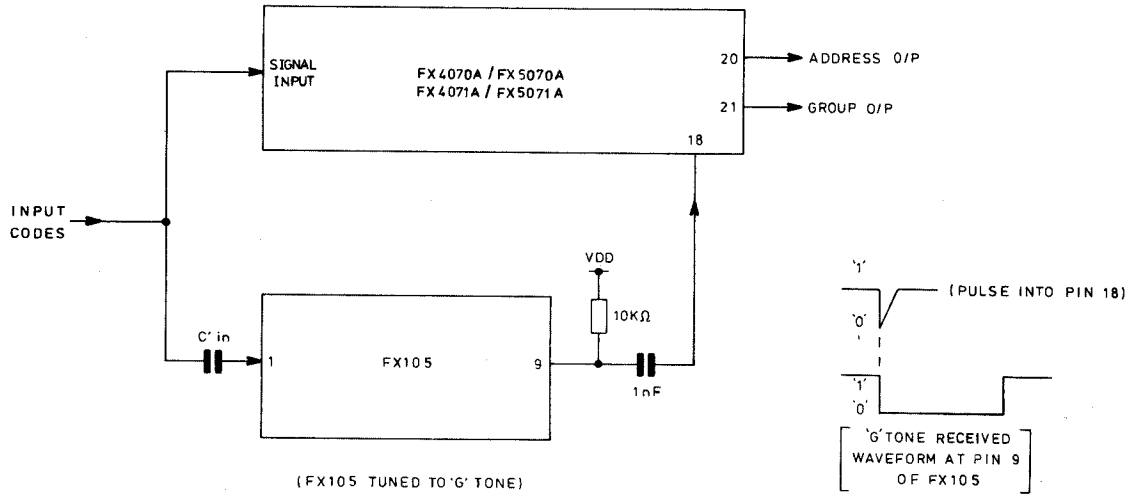
Shortened codes are achieved by linking S5 directly to the last digit.

EXAMPLES OF CODING

SEQUENCE OUTPUTS	S1 S2 S3 S4 S5	S1 S2 S3 S4 S5	S1 S2 S3 S4 S5	S1 S2 S3 S4 S5
PROGRAMMING LINKS	↓ ↓ ↓ ↓ ↓	↓ ↓ ↓ ↓ ↓	↓ ↓ ↓ ↓ ↓	↓ ↓ ↓ ↓ ↓
DIGIT INPUTS	2 0 9 6 4	2 1 R 0	1 5 6 9	3 6 5
PROGRAMMED ADDRESS	2 0 9 6 4	2 1 1 1 0	1 5 6 9 6	3 6 5

GROUP CALLING

CIRCUIT ARRANGEMENT



When an input code contains a 'G' tone, the FX105 switches ON and the 1→0 edge is coupled to the Group Initiate input (pin 18) of the hybrid. This causes the hybrid to change from the Address code programmed, to an internal Group programme for the remaining digits of the input code. If the Group code is correctly completed, the Group output of the hybrid switches ON. The Group Initiate is effective only if the correct first two digits of the Address code have been received. The Group Initiate input is disabled during transmit mode, a Group call is transmitted by encoding the 'G' tone via the Digit Select inputs.

EXAMPLES OF GROUP CALLING

INPUT CODE	ACTIVATES RECEIVERS CODED:	GROUPS OF:	O/P SWITCHED
25784	25784 only	1	ADDRESS
2578G	25780 to 25789	10	GROUP
257GR	25700 to 25799	100	GROUP
25GRG	25000 to 25999	1000	GROUP