

CML Semiconductor Products

PRODUCT INFORMATION

FX439 FFSK Modem

With compliments of Island Labs

- Features
- 1200 Baud FFSK Modem
- Meets Cellular and Trunked Radio Specifications
- Full-Duplex 1200 Baud
- On-Chip Rx and Tx Bandpass Filters
- Clock Recovery and Carrier Detect Facilities
- Pin Selectable Xtal/Clock Frequencies (1.008MHz or 4.032MHz Input)

Publication D/439/1 August 1988 Provisional Issue

Applications

- Mobile and Cellular Radio Data Signalling
- NMT 450/900
- Band III
- Radiocom 2000
- ZVEI
- Personal Radio
- Portable Data Terminals
- General Purpose Applications



Brief Description

The FX439 is a single-chip CMOS LSI circuit which operates as a 1200 baud FFSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing fullduplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, Tx and Rx synchronization are all derived from a highly stable Xtal oscillator. The onchip oscillator is capable of working at one of two input frequencies, from a 1.008MHz or 4.032MHz external Xtal/clock input, frequency being pin selectable with the 'Clock Rate' logic input. The device includes circuitry for carrier detect and facility for the Rx clock recovery. An on-board switched capacitor 900Hz — 2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analogue filters and digital signal processing results in excellent dynamic performance with few external components, the CMOS process and current saving techniques offer low standby supply current for portable battery powered applications.

Pin Number Function

DIL FX439J	Quad FX439LG	Quad FX439LH			
1	1	1	Xtal/Clock : The input to an on-chip inverter for use with either a 1.008MHz or a 4.032MHz Xtal. Alternatively, an external clock may be used. Xtal frequency selection is selectable on the 'Clock Rate' input pin.		
2	2	2	Xtal: Output of on-chip inverter. (See Figure 2).		
3	3	4	Tx Sync O/P: A 1200Hz squarewave used to synchronize the input of logic data and transmission of the FFSK signal <i>(See Figure 5)</i> .		
5	5	7	Tx Signal O/P: With the transmitter disabled, this pin is set to a high impedance state. When the transmitter is enabled, this pin outputs the 1200/1800Hz (140 step pseudo sinewave) FFSK signal (<i>See Figure 5</i>).		
6	7	9	Tx Data I/P: Serial logic data to be transmitted, is input to this pin and synchronized by the "Tx Sync O/P" (See Figure 5).		
7	8	10	Tx Enable: A logic '1' applied to this input will put the transmitter into powersave whilst forcing ''Tx Sync O/P'' to a logic '1' and ''Tx Signal O/P'' to a high impedance state. A logic '0' will enable the transmitter (<i>See Figure 5</i>). This pin is internally pulled to V_{DD} .		
8	9	11	Bandpass O/P: This is the output of the Rx 900Hz -2100 Hz bandpass filter. The output impedance of this pin is typically $10k\Omega$ and may require buffering prior to use.		
9	10	12	Rx Enable: A logic '0' applied to this input will put the receiver into powersave whilst forcing "Clocked Data O/P" and "Carrier Detect" to logic '0'. A logic '1' will enable the receiver "Rx Sync Out" may be a logic '1' or '0' during powersave. This pin is internally pulled to V_{DD} .		
10	11	13	Bias: Provides bias internally and should be decoupled externally to V_{SS} by a capacitor (C ₂). (See Figure 2).		
11	12	14	V _{ss} : Negative supply rail (GND).		
12	13	15	Unclocked Data O/P: This pin outputs recovered asynchronous serial data from the receiver.		
13	14	16	Clocked Data O/P: This pin outputs recovered synchronous serial data from the receiver and is internally latched out by a recovered clock appearing on the "Rx Sync O/P" pin (<i>See Figure 6</i>).		
14	15	17	Carrier Detect O/P: This pin will output a logic '1' when an FFSK signal is being received.		
15	16	20	Rx Signal I/P: This is the FFSK signal input pin for the receiver and should be decoupled via a capacitor C_3 .		
17	18	22	Rx Sync O/P: This is a flywheel 1200Hz squarewave output which upon presentation of FFSK data signal is synchronised internally to the incoming data (<i>See Figure 6</i>).		
19	21	25	Clock Rate: This logic input selects and allows the use of either a 1.008MHz or 4.032MHz Xtal/clock input to the on-chip inverter. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).		
20	22	27	Carrier Detect Time Constant (τ): This input forms part of the carrier detect integration function. The value of C ₄ connected to this pin will affect the carrier detect response time and hence noise performance (<i>See Figure 2, Note 3</i>).		
22	24	28	V _{DD} : Positive supply rail. A single 5-volt supply is required.		
4, 16, 18, 21	4, 6, 17, 19, 20, 23	3, 5, 6, 8, 18, 19, 21, 23, 24, 26	No Connection: These pins are open circuit, do not connect to.		
			Note: Output Loading. Large capacitive loads could cause the output pins of this device to oscillate. If capacitive loads in excess of 200pF are unavoidable, a resistor of typically 100 Ω put in series with the load should minimise this effect.		



Fig. 2 External Component Connections



Fig. 3 Typical Variation of 'B.E.R.' with Input Signal Level



Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3V to 7.0V
Input voltage at any pin (ref)	$V_{SS} = OV$	$-0.3V$ to $(V_{DD} + 0.3V)$
Output sink/source current (1	total)	20mA
Operating temperature range	: FX439J	-30° C to $+85^{\circ}$ C (cerdip)
	FX439LG/LH	-30° C to $+70^{\circ}$ C (plastic)
Storage temperature range:	FX439J	$-55^{\circ}C$ to $+125^{\circ}C$ (cerdip)
	FX439LG/LH	-40° C to $+85^{\circ}$ C (plastic)
Total device dissipation @ T	MB 25°C	800mW Max.
Derating		10mW/°C

Operating Limits

All characteristics measured using the standard test circuit (Figure 4) with the following test parameters and is valid for all tests unless otherwise stated:

 $V_{DD} = +5V$, $T_{amb} = 25^{\circ}C$, Xtal (X₁) Frequency: 1.008MHz **OdB** reference

Noise

SNR ratio measured in bit rate bandwidth (1200Hz)

300mV rms (band limited 5kHz gaussian white noise)

Characteristics	See Note	Min.	Тур.	Max.	Unit
Static Characteristics					
Supply Volts		4.5	5.0	5.5	V
Supply Current: Rx (Enabled) Tx (Disabled)	-	3.6		mA
Rx (Enabled) Tx (Enabled)		-	4.5	-	mA
Rx (Disabled) Tx (Disabled)	-	650	12	μA
Logic '1' level		80%Vpp		_	V
Logic '0' level		_	-	20%V	v
Digital Output Impedance		_	4	_	kΩ
Analogue and Digital Input Impedance		100	2		kΩ
Tx Output Impedance		_	10		kΩ
On-Chip Crystal Oscillator:					
R.		10	-	_	MΩ
B		5	_	15	kΩ
Inverter Gain		10	_	20	dB
Gain Bandwidth Product		3 x 10 ⁶	_	_	db
Crystal Frequency	1	_	1.008		MHz
Crystal Frequency	1	_	4.032	_	MHz
Dynamic Characteristics					
Receiver:					
Signal Input: Dynamic Range (50dB SNR)	2.3	100	230	1000	mV rms
Bit Error Rate: 12dB SNR	3	_	7.0	_	10-4
20dB SNR	3	_	1.0		10-8
Receiver Synchronization 12dB SNR:	6		0.00		** *
Probability of Bit 8 being correct			0.99		
Probability of Bit 16 being correct			0.995		
Carrier Detect	4				
Sensitivity	6, 7	_	_	100	mV rms
Probability of Carrier Detect being high:	10.00				
12dB SNR after Bit 8	4	-	0.98	_	
12dB SNR after Bit 16	4	-	0.995	_	
Transmitter Output					
Tx Output Level		-	775	—	mV rms
Output Level Variation 1200/1800Hz		0	_	±1.00	dB
Output Distortion		_	3	5	%
3rd Harmonic Distortion		_	2	3	%
Logic '1' Carrier Frequency	5	<u> </u>	1200	_	Hz
Logic '0' Carrier Frequency	5	-	1800	_	Hz
Isochronous Distortion			12,202,007		
1200Hz – 1800Hz		-	25	40	μs
1800Hz - 1200Hz		—	20	40	μs

Notes: 1. Crystal frequency, type and tolerance depends on system requirements. 2. See Figure 3.

3. SNR (Bit Rate Bandwidth).

4. See Figure 2 Note 3.

5. Depending on crystal tolerance. 6. 10101010101 . . . pattern.

7. Measured with 100mV rms signal (No noise).











Fig. 6 Receiver Timing Diagram

Package Outlines

The FX439J, the cerdip package, is illustrated in *Figure 8*. The 'LG' version is shown in *Figure 9* and the 'LH' version in *Figure 10*. To allow complete identification, the FX439 'LG' and 'LH' packages have an indent spot adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 for LG package, between Pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).

Fig. 8 FX439J DIL Package



Ordering Information

FX439J	22-pin cerdip DIL		
FX439LG	24-pin quad plastic		
	encapsulated, bent and		
	cropped.		
FX439LH	28-lead plastic leaded chip		
	carrier.		
	ESCO VENETO s.r.l.		
	Viale Mazzini, 131		
	36100 VICENZA		
	Tel. 0444/546355 - 546010		
	Fax 0444/547399		

Handling Precautions

The FX439J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

Fig. 9 FX439LG Package



Fig. 10 FX439LH Package



CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.



CONSUMER MICROCIRCUITS LIMITED

WITHAM — ESSEX CM8 3TD — ENGLAND © 1988 Consumer Microcircuits Limited Telephone: (0376) 513833 Telex: 99382 CMICRO G Telefax: (0376) 518247