FX805 Sub-Audio Signalling Processor
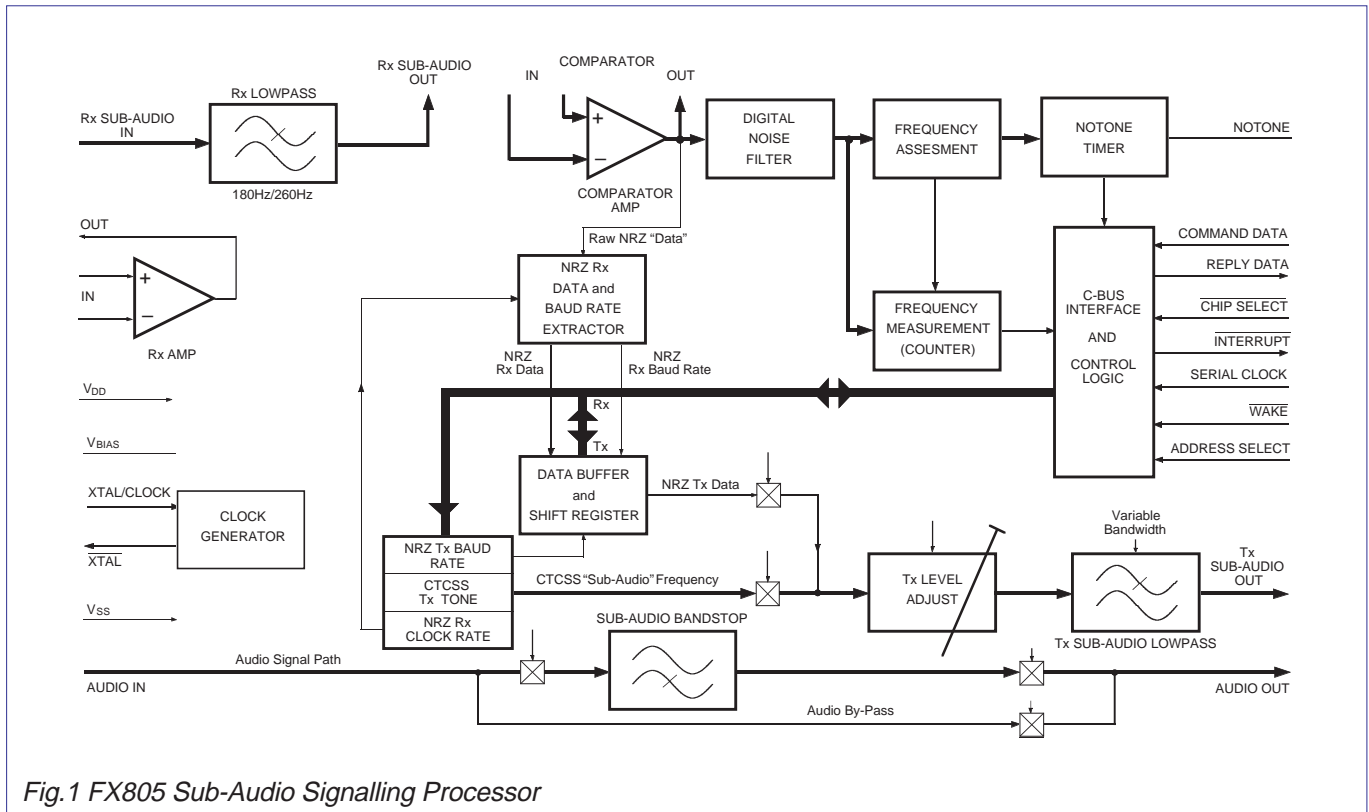
Island Labs

Fig.1 FX805 Sub-Audio Signalling Processor

FX805 Sub-Audio Signalling Processor

A μProcessor controlled, sub-audio frequency signalling processor to provide an outband audio and digital signalling facility for PMR radio systems.

This device caters for the transmission and non-predictive reception of:

- *Continuous Tone Controlled Squelch (CTCSS) tones and other non-standard sub-audio frequencies.*

- *Non-Return-to-Zero (NRZ) data to facilitate Continuous Digitally Coded Squelch (CDCS/DPL™) system operations.*

To achieve these functions, the FX805 has on-chip:

- *A non-predictive CTCSS Tone Decoder and CDCS sub-audio signal demodulator.*

- *A CTCSS/NRZ Encoder with Tx level adjustment and lowpass filter output stage with optional NRZ pre-emphasis.*

- *A selectable sub-audio bandstop filter.*

- *A Notone (CTCSS Rx) period timer.*

Setting of the FX805 functions and modes is by data loaded from the μController to the controlling registers within the device. Reply Data and Interrupt protocol keep the μController up to date on the operational status of the circuitry — all via the "C-BUS" interface.

CTCSS tone data for transmission is generated within the μController, loaded to CTCSS Tx Frequency Register, encoded and output as a tone via the Tx Sub-Audio Lowpass Filter.

Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data-word, is presented via the CTCSS Rx Frequency Register to the μController for matching against a 'look-up' table. Noise filtering is provided to improve the signal quality prior to measurement.

NRZ coded data streams for transmission, when generated within a μController, are loaded to the NRZ Tx Data Buffer and output, in 8-bit bytes, through the Lowpass Filter circuitry as sub-audio signals. CDCS turn-off tones can be added to the data signals by switching the FX805 to the CTCSS transmit mode at the appropriate time.

NRZ coding is produced by the μController and translated into sub-audio signals by the FX805.

Received NRZ data is filtered, detected and placed into the NRZ Rx Data Register which is then available for transfer one byte at a time, to the μController, for decoding by software. Clock extraction circuitry is provided on chip and Rx and Tx baud rates are selectable.

Provision is made in both hardware and system software allocations to address two FX805 Sub-Audio Signalling Processors consecutively to achieve multi-mode, duplex operation.

The FX805 has a powersaving function which may be controlled by software or a dedicated (Wake) input.

The FX805 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/lead plastic SMD packages.

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Pin Number Function

FX805 J/LG/LS	
1	**$\overline{Xtal}$:** The output of the on-chip clock oscillator. External components are required at this input when a Xtal (f_{XTAL}) input is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock (f_{XTAL}) should be connected here. See Figure 2.
3	**Address Select:** This pin enables two FX805 devices to be used on the same "C-BUS," providing full-duplex operation. See Tables 1 and 2.
4	**Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the µController, by going to a logic "0." This is a "wire-or able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The System $\overline{IRQ}$ line requires 1 pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register (Table 4) and are shown below: *Rx CTCSS Tone Measurement Complete* *CTCSS NOTONE Timer Expired* *1 NRZ Rx Data Byte Received* *New NRZ Rx Data Received Before Last Byte Read* *NRZ Tx Buffer Ready* *NRZ Data Transmission Complete*
5	**Serial Clock:** The "C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the Sub-Audio Signalling Processor. See Timing Diagrams.
6	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
7	**Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams.
8	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{Chip\ Select}$ input. This 3-state output is held at high impedance when not sending data to the µController. See Timing Diagrams.
9	**Tx Sub-Audio Out:** The sub-audio output (pure or NRZ derived). Signals are band-limited, the Tx Output Filter has a variable bandwidth, see Table 6. This output is at V_{BIAS} (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the FX805 is placed in the Powersave All condition.
10	**Audio In:** The input to the switched sub-audio bandstop (highpass) filter. This input is internally biased and requires to be a.c. coupled by capacitor C_7.
11	**Audio Out:** The output of the 'audio signal path' (filter or by-pass). This output is controlled by the Control Register and when disabled is held at $V_{DD}/2$.
12	**V_{SS}:** Negative Supply (Signal Ground).

Pin Number Function

FX805 J/LG/LS	
13	**Rx Amp (-) In:** The inverting input to the on-chip Rx Input Amp. See Figures 2, 3 and 4.
14	**Rx Amp (+) In:** The non-inverting input to the on-chip Rx Input Amp.
15	**Rx Amp Out:** The output of the on-chip Rx Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and an anti-aliasing filter prior to the Rx Lowpass Filter, or for other purposes. See Figure 2 for component details.
16	**Rx Sub-Audio In:** The received sub-audio (CTCSS/NRZ) input. This input is internally biased to $V_{DD}/2$ and requires to be a.c. coupled or biased. See Figure 2 for component details.
17	**Rx Sub-Audio Out:** The output of the Rx Lowpass Filter. This output may be coupled into the on-chip amplifier or comparator as required.
18	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by capacitor C_8 (see Figure 2).
19	**Comparator In (-):** The inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
20	**Comparator (+):** The non-inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
21	**Comparator Out:** The output of the "comparator" amplifier. This node is also internally connected to the input of the Digital Noise Filter (see Figure 1). When both decoders are Powersaved, this output is at a logic "0."
22	**NOTONE Timing:** External RC components connected to this pin form the timing mechanism of a NOTONE period timer. The external network determines the 'charge-rate' of the timer to $V_{DD}/2$. Expiry of the timer will cause an interrupt. This facility is only used in the CTCSS Rx mode.
23	**Wake:** This 'real-time ' input can be used to reactivate the FX805 from the 'Powersave All' condition using an externally derived signal. The FX805 will be in a 'Powersave All' condition when both this pin and Bit 0 of the Control Register are set to a logic "1." Recovery from "Powersave All" is achieved by putting either the Wake pin or the 'Powersave All' bit to logic "0," thus allowing FX805 activation by the μController or an external signal, such as R.S.S.I. or Carrier Detect.
24	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within the Sub-Audio Signalling Processor are dependant upon this supply.

NOTE: (i) Further information on external components and DBS 800 system integration of this microcircuit are contained in the System Support Document.
(ii) A glossary of abbreviations used in this document is supplied.
(iii) Guidance upon the generation and manipulation of NRZ Rx and Tx data is given in DBS 800 Application Support Document.

"C-BUS" is CML's proprietry standard for the transmission of commands and data between a μController and DBS 800 microcircuits. It may be used with any μController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of μController. The "C-BUS" data rate is determined soley by the μController.
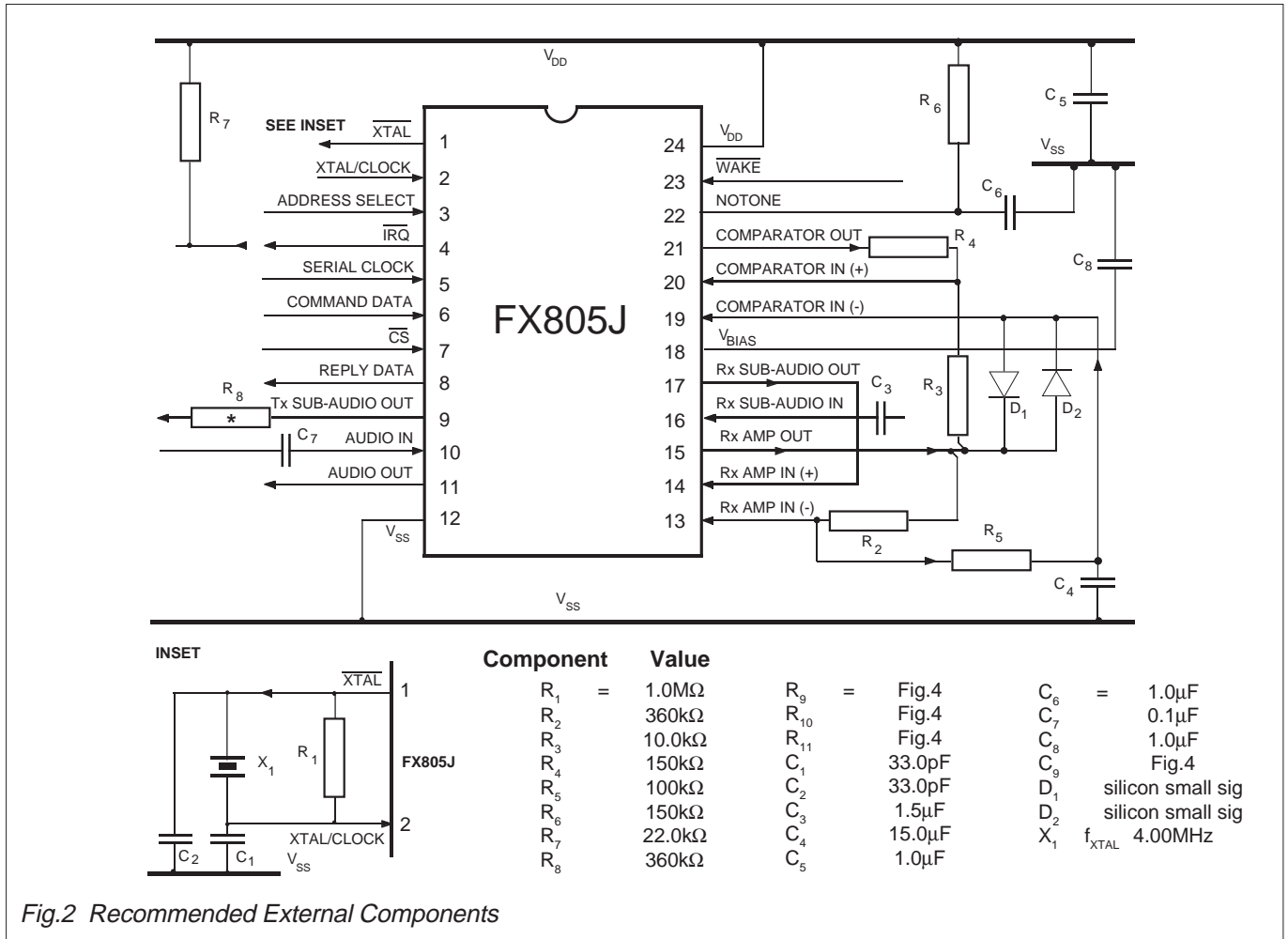
Application Information

External Components

Fig.2 Recommended External Components

Component		Value						
R_1	=	1.0MΩ	R_9	=	Fig.4	C_6	=	1.0µF
R_2		360kΩ	R_{10}		Fig.4	C_7		0.1µF
R_3		10.0kΩ	R_{11}		Fig.4	C_8		1.0µF
R_4		150kΩ	C_1		33.0pF	C_9		Fig.4
R_5		100kΩ	C_2		33.0pF	D_1		silicon small sig
R_6		150kΩ	C_3		1.5µF	D_2		silicon small sig
R_7		22.0kΩ	C_4		15.0µF	X_1	f_{XTAL}	4.00MHz
R_8		360kΩ	C_5		1.0µF			

Notes *on external components and connections*

1. Xtal/clock circuitry components shown INSET are recommended in accordance with CML Application Note D/XT/2 December 1991. The DBS 800 System Information Document contains additional notes on Xtal/clock distribution and frequencies.

2. R_8 is a System Component. Its value is chosen, for example, with the FX806 Modulation Summing Amplifier, to provide a sub-audio signal level of -11.0dB to the system modulator.

3. Components R_6 and C_6 are NOTONE timing components.

4. R_2 and R_5 are dependant upon the input signal level. Values given are for the specified composite signal.

5. R_7 is used as the DBS 800 system common-pullup for the "C-BUS" Interrupt Request (IRQ) line, the optimum value of this component will depend upon the circuitry connected to the IRQ line.
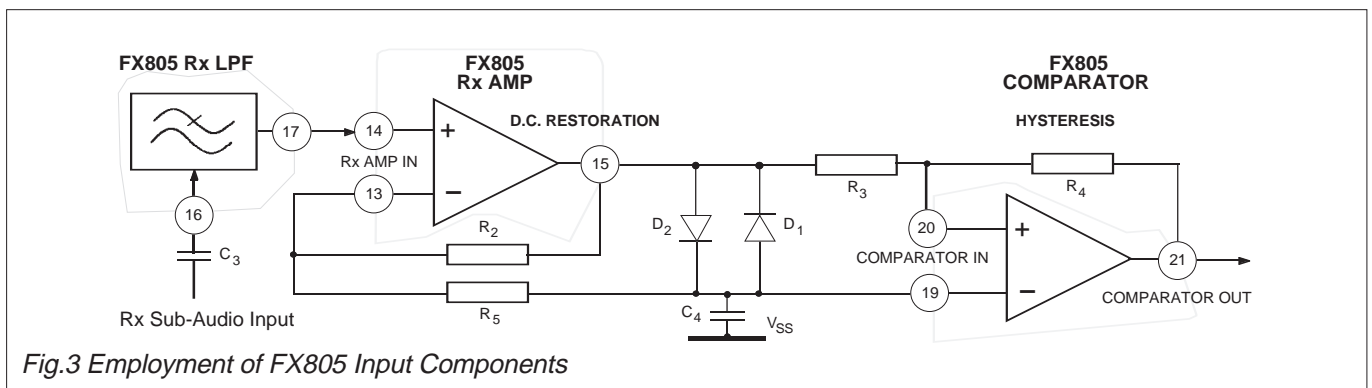

Fig.3 Employment of FX805 Input Components

With reference to Figure 2, Figures 3 and 4 show in detail recommended alternative component configurations for the FX805.

Application Information ......

External Components ......

Figure 3 shows an input component configuration for use generally for CTCSS signal and NRZ data reception.

Input coupling capacitor C_3 is required because the Rx Sub-Audio Input is held at V_{BIAS} during all powered conditions of the FX805. Diodes D_1 and D_2 can be any silicon small-signal diode.

The output resistance (open loop) of the on-chip Rx Amp is ≈ 6kΩ. In the configuration shown in Figure 3, the (Rx Amp) RC time-constant is therefore 90ms. If this period is too long for some systems, ie. those employing half-duplex, short data bursts, an external amplifier should be considered in place of the FX805 on-chip Rx Amp.
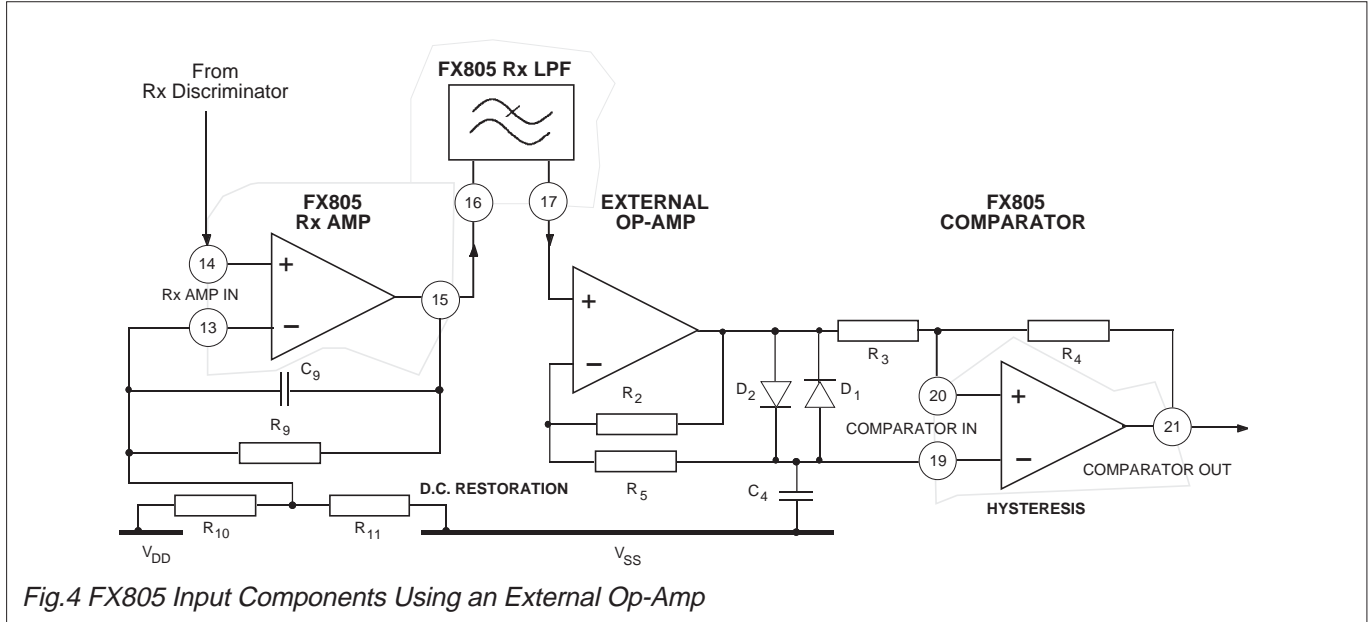

Fig.4 FX805 Input Components Using an External Op-Amp

Using an External Op-Amp

For d.c. coupling the FX805 to the receiver's discriminator output when using NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will allow long sequences of logic "1ˢ" or "0ˢ" to be successfully decoded (eg. LTR™ trunking systems).

Components R_9, R_{10} and R_{11} should be calculated to provide an accurate potential of 2.5V d.c. (equal to V_{BIAS}) at pin-junction 15/16 when using a discriminator input. C_9 is an optional component which, if additional filtering is required, should be calculated, with R_9 to provide a lowpass cut-off frequency (f_{CO}) of 500Hz.

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FX805 Operational Modes

NRZ Tx (Encoding)

The NRZ Encoder is formed by a shift register and the Tx Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ Tx Data Register. The output data-signal level may be adjusted and filtered. Data may be pre-emphasized via a "C-BUS" command. The Tx baud rate is programmed as the NRZ Tx Baud Rate ($R_{NRZ Tx}$) (Table 5).

CTCSS Tx (Encoding)

The CTCSS Tone Encoder comprises a clock-divider programmed by an 11-bit binary number (Q) loaded to the CTCSS Tx Frequency Register (Table 5) via the "C-BUS" Command Data line.

The square-wave output of the encoder is fed through the Tx Level Adjust variable gain block to the Tx Sub-Audio Lowpass Filter, a variable bandwidth circuit controlled by 4-bits (P) of the CTCSS Tx Frequency Register. The Tx Sub-Audio output is a sine-wave. Standard and non-standard sub-audio tones are available, a 'CDCS' turn-off tone may be generated.

NRZ Rx (Decoding)

Input (NRZ type) sub-audio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output one 8-bit byte at a time as Reply Data from the NRZ Rx Data Register (Page 14) to the μController. The expected Rx baud rate is programmed as the NRZ Rx Baud Rate ($R_{NRZ Rx}$) (Table 5). Any codeword recognition can be carried out by software.

CTCSS Rx (Decoding)

Received CTCSS signals are filtered, coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle-to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64 milliseconds.

If the average signal quality is consistently too low, NOTONE is indicated, if not, the input frequency is precisely indicated in the CTCSS Rx Frequency Register in a binary form as shown in Figure 6.

As any single sub-audio tone within the specified range may be selected, this would enable a 'CDCS' turn-off tone (of 134Hz) to be decoded whilst operating in the NRZ Rx mode.

Controlling Protocol

Control of the FX805 Sub-Audio Signalling Processor's operation is by communication between the µController and the FX805 internal registers on the "C-BUS," using Address/Commands (A/Cs) and appended instructions or data (see Figure 9). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select input enables the addressing of 2 separate FX805s on the "C-BUS" to provide full-duplex multi-mode signalling.

FX805 Internal Registers

FX805 internal registers are detailed below:

Control Register ($70_H/78_H$) – Write only, control and configuration of the FX805.

Status Register ($71_H/79_H$) – Read Only, reporting of device functions.

CTCSS Rx Frequency Register ($72_H/7A_H$) – Read Only, a 2-byte binary word indicating the frequency of the received sub-audio input.

CTCSS Tx Frequency / NRZ Tx or Rx Baud Rate Register ($73H/7B_H$) – Write Only, a 2-byte command to set the relevant parameters.

NRZ Rx Data Register ($74_H/7C_H$) – Read Only, a single-byte of received NRZ data.

NRZ Tx Data Register ($75_H/7D_H$) – Write Only, to load a single-byte of NRZ data for transmission one byte at a time.

Gain-Set Register ($76_H/7E_H$) – Write Only, a single byte to set the gain of the Tx Lowpass Filter.

Address/Commands

The first byte of a loaded data sequence is always recognized by the "C-BUS" as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i)   further instructions or data or,

(ii) a Status or data Reply.

Instructions and data are loaded and transferred, via "C-BUS," in accordance with the timing information given in Figures 9 and 10.

Placing the Address Select input at a logic "0" will address FX805 No.1, a logic "1" will address FX805 No.2.

Tables 1 and 2 show the list of A/C bytes relevant to the FX805. A complete list of DBS 800 "C-BUS" Address allocations is published in the System Support Document.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Control Reg.	70	0	1	1	1	0	0	0	0	+	1 byte Instruction to Control Reg.
Read Status Reg.	71	0	1	1	1	0	0	0	1	+	1 byte Reply from Status Reg.
Read CTCSS Rx Freq. Reg.	72	0	1	1	1	0	0	1	0	+	2 byte Reply of CTCSS Rx data
Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg.	73	0	1	1	1	0	0	1	1	+	2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	74	0	1	1	1	0	1	0	0	+	1 byte binary data Reply
Write to NRZ Tx Data Reg.	75	0	1	1	1	0	1	0	1	+	1 byte binary data Command
Write to Gain-Set Reg.	76	0	1	1	1	0	1	1	0	+	1 byte Instruction for Tx Output

Table 1 – FX805 No.1 "C-BUS" Address/Commands   Address Select input at a logic "0"

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB							LSB	+	Data Byte/s
General Reset	01	0	0	0	0	0	0	0	1		
Write to Control Reg.	78	0	1	1	1	1	0	0	0	+	1 byte Instruction to Control Reg.
Read Status Reg.	79	0	1	1	1	1	0	0	1	+	1 byte Reply from Status Reg.
Read CTCSS Rx Frequency Reg.	7A	0	1	1	1	1	0	1	0	+	2 byte Reply of CTCSS Rx data
Write to CTCSS Tx Frequency/ NRZ Baud Rate Reg.	7B	0	1	1	1	1	0	1	1	+	2 byte Instruction for Tx Frequency and NRZ Tx/Rx baud rates
Read NRZ Rx Data Reg.	7C	0	1	1	1	1	1	0	0	+	1 byte binary data Reply
Write to NRZ Tx Data Reg.	7D	0	1	1	1	1	1	0	1	+	1 byte binary data Command
Write to Gain-Set Reg.	7E	0	1	1	1	1	1	1	0	+	1 byte Instruction for Tx Output

Table 2 – FX805 No.2 "C-BUS" Address/Commands   Address Select input at a logic "1"

Controlling Protocol ......

"Write to Control Register" – A/C 70$_H$ (78$_H$), followed by 1 byte of Command Data.

Table 3 (below) shows the configurations available to the FX805. Bits 5, 6 and 7 are used together to Enable and Powersave circuit sections as required.

Setting			Control Bits	
MSB			**Transmitted First**	
7	**6**	**5**	**Functions Enabled**	**Functions Powersaved**
0	0	0	CTCSS Decoder	NRZ Decoder and Both Encoders
0	0	1	NRZ Decoder	CTCSS Decoder and Both Encoders
0	1	0	CTCSS Encoder	All Decoders
0	1	1	NRZ Encoder	All Decoders
1	0	0	CTCSS Encoder and Decoder	NRZ Encoder and Decoder
1	0	1	NRZ Encoder and CTCSS Decoder	None
1	1	0	NRZ Decoder and CTCSS Decoder	All Encoders
1	1	1	NRZ Decoder	All Encoders (except Tx Sub-Audio LPF) and CTCSS Decoder
4				
1			Enable Audio Output – Used with Bit 3	
0			Disable Audio Output – Output to V$_{BIAS}$	
3				
1			Enable Sub-Audio Bandstop Filter (Audio Signal Path)	
0			By-pass Sub-Audio Bandstop Filter	
2				
1			Enable All FX805 Interrupts	
0			Disable All FX805 Interrupts	
1				
1			Set Rx Lowpass Filter bandwidth to 180Hz – For low CTCSS Tones or NRZ Data	
0			Set Rx Lowpass Filter bandwidth to 260Hz	
0				
1			All Encoders and Decoders Powersaved (Powersave All)	
0			All Encoders and Decoders Enabled unless individually Powersaved	

Table 3 Control Register

General Reset

Upon Power-Up the "bits" in the FX805 registers will be random (either "0" or "1"). A General Reset Command (01$_H$) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX805.

Control Register	*Set as 00$_H$*
Status Register	*Set as 00$_H$*
N$_{OTONE}$ Timer	*Discharged*

Warning – The following FX805 register configurations are not affected by a General Reset command:
   CTCSS Rx Frequency
   CTCSS Tx Frequency/NRZ Baud Rate Register
   NRZ Rx Data Register
   NRZ Tx Data Register
   Gain-Set Register

Note that setting the Control Register in this way (General Reset) will set the FX805 to the CTCSS Decode mode and overwrite a "Powersave All" instruction.

It should also be considered that a General Reset command will reset ALL DBS 800 microcircuits operating on the "C-BUS."

Glossary of Abbreviations

Below is a list of abbreviations used within this Data Sheet.

CDCS	Continuous Digitally Coded Squelch
CTCSS	Continuous Tone Controlled Squelch
DPL™	Digital Private Line
LTR™	Logic Trunked Radio
NRZ	Non-Return-to-Zero data levels
f$_{CO}$	Filter cut-off frequency
f$_{CTCSS\ IN}$	Sub-Audio Rx frequency
f$_{CTCSS\ OUT}$	Sub-Audio Tx frequency
f$_{TONE}$	Tone frequency
f$_{XTAL}$	Xtal/clock frequency
R$_{NRZ\ Rx}$	NRZ Rx baud rate
R$_{NRZ\ Tx}$	NRZ Tx baud rate
S$_{INPUT}$	Audio input signal

Controlling Protocol ......

"Read Status Register" – A/C 71$_H$ (79$_H$), followed by 1 byte of Reply Data.

The Status Register indicates the operational condition of the FX805. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status Bit is set to a logic "1," an Interrupt Request ($\overline{IRQ}$) output is generated. A read of the Status Register will reset the interrupt condition and ascertain the state of this register.

Table 4 (below) shows the conditions indicated by the Status Bits.

Status Bit	Set By	Logic	Cleared By	Logic
MSB **7 , 6**	**Received First** Not used	"0"	Not used	"0"
5	NRZ data transmission complete. No new data loaded.	"1"	1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Encoder Powersave.	"0"
4	NRZ Tx Data Buffer ready for next data byte.	"1"	1. Write to NRZ Tx Data Reg. or, 2. General Reset or, 3. NRZ Tx Powersave.	"0"
3	New NRZ Rx data received **before** last byte was read.	"1"	1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave.	"0"
2	1 byte of NRZ Rx data received.	"1"	1. Read NRZ Rx Data Reg. or, 2. General Reset or, 3. NRZ Decoder Powersave.	"0"
1	N$_{OTONE}$ Timer period expired.	"1"	1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave.	"0"
0	Rx Tone Measurement complete.	"1"	1. Read Status Register or, 2. General Reset or, 3. CTCSS Decoder Powersave.	"0"

Table 4 Status Register

"Read CTCSS Rx Frequency Register" – A/C 72$_H$(7A$_H$), followed by 2 bytes of Reply Data.
Measurement of CTCSS Rx Frequency (f$_{CTCSS IN}$)

The input sub-audio signal (f$_{CTCSS IN}$), is filtered and measured in the Frequency Counter over the "measurement period" (122.64ms).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the measurement period of a successful decode is complete, the Rx Tone Measurement bit in the Status Register, and the Interrupt bit are set.

The CTCSS Rx Frequency Register will now indicate the sub-audio signal frequency (f$_{CTCSS IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.
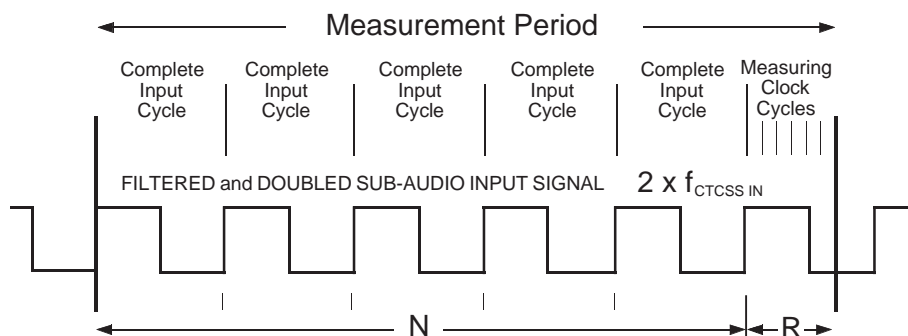

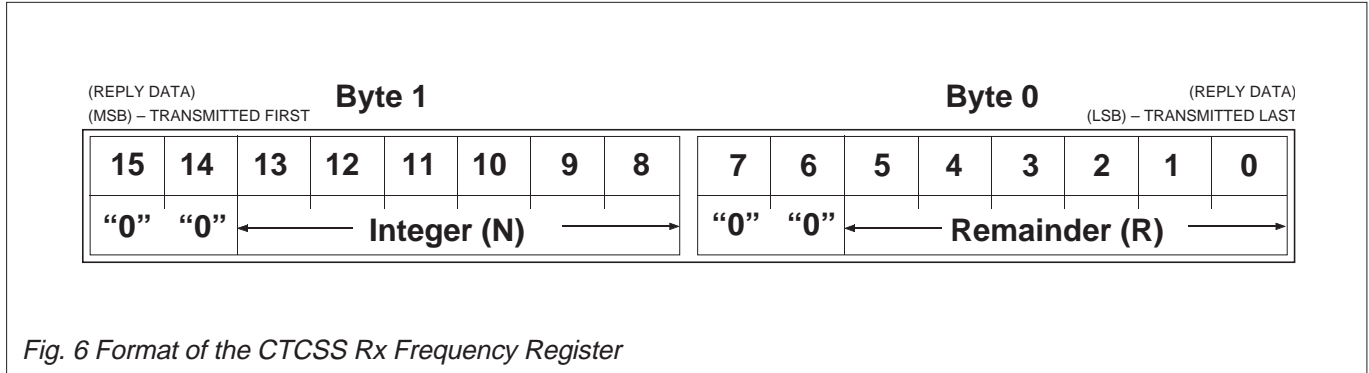*Fig.5 Measurement of a CTCSS Rx Frequency*

Controlling Protocol ......

"Read CTCSS Rx Frequency Register" ......

The Integer (N) – Byte 1

A binary number representing 'twice the number of complete input sub-audio cycle periods' counted during the measurement period of 122.64ms

The Remainder (R) – Byte 0

A binary number representing the remainder part, R, of 2 x Sub-Audio Input Frequency. 'R = number of specified measuring-clock cycles' required to complete the specified measurement period (See N). The clock-cycle frequency is 4166.6Hz

(REPLY DATA) (MSB) – TRANSMITTED FIRST	**Byte 1**							**Byte 0**							(REPLY DATA) (LSB) – TRANSMITTED LAST
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
"0"	"0"	←		Integer (N)			→	"0"	"0"	←		Remainder (R)			→

Fig. 6 Format of the CTCSS Rx Frequency Register

CTCSS Rx Frequency Register

Figure 6 (above) shows the format of the CTCSS Rx Frequency Register.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of N = $16 \leq N \leq 61$.

ie. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) (Byte 0) are used to represent the Remainder (R). From Byte 0, valid values of R = ≤ 31.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

CTCSS Rx Frequency Measurement Formulæ

To assist in the production of 'look-up' tables and limit-values in the µController and provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulæ show the derivation of the CTCSS Rx Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

$f_{CTCSS\ IN}$

In the measurement period of 122.64ms there are N cycles at 2 x $f_{CTCSS\ IN}$ and R clock-cycles at 4166.6Hz, for any input frequency.

So

$$f_{CTCSS\ IN} = \frac{N \times f_{XTAL}}{1920 \times (511 - R)} \ \text{Hz} \quad [1] \qquad R = INT\left[511 - \left[\frac{N \times f_{XTAL}}{1920 \times f_{CTCSS\ IN}}\right] + 0.5\right] \quad [3]$$

$$N = INT\left[\frac{(1920 \times 511 \times f_{CTCSS\ IN})}{f_{XTAL}}\right] \quad [2]$$

Calculate N first

Examples (f_{XTAL} = 4.00MHz)**:** $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

NOTONE Timing

The input sub-audio signal is monitored by the Frequency Assessment circuitry. Before any NOTONE action is enabled, the FX805 must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the NOTONE Timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (NOTONE Timer Expired) are generated. This is a one-shot function and is reset by a "Tone Measurement Complete" interrupt.

Controlling Protocol ......

"Write to CTCSS Tx Frequency/NRZ Baud Rate Register" – A/C 73_H ($7B_H$), followed by 2 bytes of Command Data.

The information loaded to this register will set either the:

    (a) CTCSS Tx Tone Frequency $f_{CTCSS\ OUT}$

    (b) NRZ Tx Baud Rate $R_{NRZ\ Tx}$

    (c) NRZ Rx Baud Rate $R_{NRZ\ Rx}$

The chosen mode for this register (a, b or c) is determined by the FX805 operational mode enabled by the Control Register (Table 3), as shown in the table below.

| Control Register Bits | | | FX805 Mode | CTCSS Tx/NRZ Baud Rate |
7	6	5	Enabled	Register Function
0	0	0	CTCSS Decode	
0	0	1	NRZ Decode	NRZ Rx Baud Rate
0	1	0	CTCSS Encode	CTCSS Tx Frequency
0	1	1	NRZ Encode	NRZ Tx Baud Rate
1	0	0	CTCSS Encode and Decode	CTCSS Tx Frequency
1	0	1	NRZ Encode and CTCSS Decode	NRZ Tx Baud Rate
1	1	0	NRZ and CTCSS Decode	NRZ Rx Baud Rate
1	1	1	NRZ Decode	NRZ Rx Baud Rate

Table 5 CTCSS Frequency/NRZ Baud Rate Register Configurations

Data Format

Data is transmitted, via "C-BUS," to this register as 2 bytes of Command Data (1 and 2) distributed as command words P and Q, in the form illustrated in Figure 7. This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.
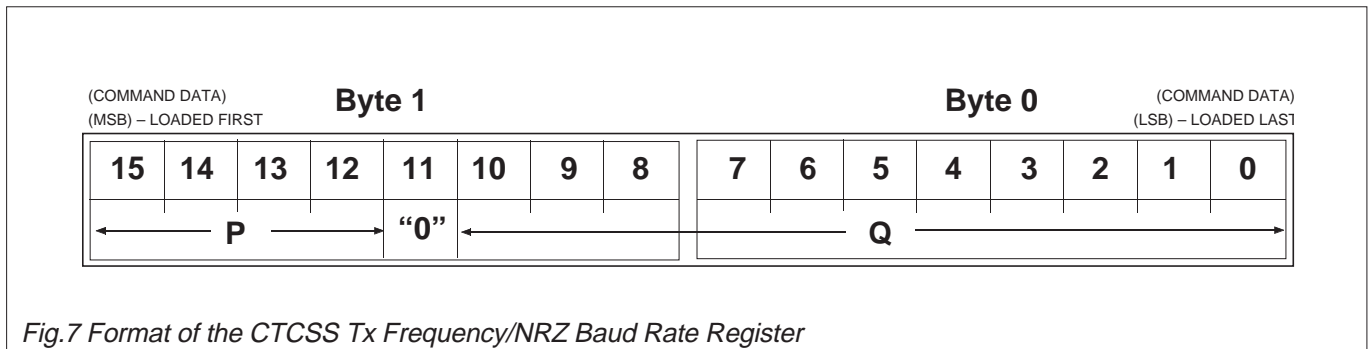

Fig.7 Format of the CTCSS Tx Frequency/NRZ Baud Rate Register

Command Words P and Q

With reference to Figure 7, the two data words, P and Q, loaded to this register are interpreted as:

P = a binary number to set the Tx Sub-Audio Lowpass Filter bandwidth (applicable to NRZ Encode and CTCSS Encode modes).

Q = a binary number to set the frequency or baud rate of the selected function (see Table 5).

Command Word 'P'

| Bits | | | LSB | | |
15	14	13	12	'P'	LPF Bandwidth
0	0	1	0	2	300Hz
0	0	1	1	3	200Hz
0	1	0	0	4	150Hz
0	1	0	1	5	120Hz
0	1	1	0	6	100Hz
0	1	1	1	7	85.7Hz
1	0	0	0	8	75Hz

Table 6 Valid Values of 'P'

Bits 12 to 15 are used to produce the data word 'P' as shown in Table 6 (left). The cut-off frequency f_{CO} (0.5dB point) of the Tx Sub-Audio Lowpass Filter is calculated as:

$$f_{CO} = \frac{f_{XTAL}}{32 \times 208.33 \times \textbf{'P'}}$$

$$so\ \textbf{'P'} = \frac{f_{XTAL}}{32 \times 208.33 \times f_{CO}}$$

Table 6 is given as an example and calculated using a Xtal/clock (f_{XTAL}) frequency of 4.00MHz. As illustrated, only values of 'P' of *2 to 8* are usable.

Controlling Protocol ......

"Write to CTCSS Tx Frequency/NRZ Baud Rate Register" ......

Command Word 'Q'

   With reference to Figure 7, Bits 0 to 10 are used to produce the data word '**Q**' which sets one of the parameters described below. As can be seen, command word '**Q**' could be used to produce a word whose value would produce a parameter outside that specified, care should be taken not to do this. Examples for limits of '**Q**' in each operational configuration are included. '**Q**' = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0".

(a)   CTCSS Tx Tone Frequency ($f_{CTCSS\ OUT}$)   **Example Limits**

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times 'Q'} \quad Hz$$

$$so\ 'Q' = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}} \quad Hz$$

$f_{CTCSS\ OUT}$ =	67Hz	
so '**Q**' =	1866	"11101001010"
$f_{CTCSS\ OUT}$ =	250Hz	
so '**Q**' =	500	"00111110100"

(b) NRZ Tx Baud Rate ($R_{NRZ\ Tx}$)

$$R_{NRZ\ Tx} = \frac{f_{XTAL}}{32 \times 'Q'} \quad bits/sec$$

$$so\ 'Q' = \frac{f_{XTAL}}{32 \times R_{NRZ\ Tx}}$$

$R_{NRZ\ Tx}$ =	67 bits/sec	
so '**Q**' =	1866	"11101001010"
$R_{NRZ\ Tx}$ =	300 bits/sec	
so '**Q**' =	417	"00110100001"

(c) NRZ Rx Baud Rate ($R_{NRZ\ Rx}$)

$$R_{NRZ\ Rx} = \frac{f_{XTAL}}{32 \times 11 \times 'Q'} \quad bits/sec$$

$$so\ 'Q' = \frac{f_{XTAL}}{352 \times R_{NRZ\ Rx}}$$

$R_{NRZ\ Rx}$ =	100 bits/sec	
so '**Q**' =	114	"00001110010"
$R_{NRZ\ Rx}$ =	300 bits/sec	
so '**Q**' =	38	"00000100110"

Controlling Protocol ......

"Read NRZ Rx Data Register" – A/C 74$_H$ (7C$_H$), followed by 1 byte of Reply Data.

Received NRZ data bits are organized into bytes and made available to the µController via the Reply Data line. As 8 bits are received into this register an interrupt is generated to indicate that a complete byte has been received, this byte must be read before the arrival of the last (8th) bit of the next incoming byte, if this is not done, an interrupt to indicate this condition will be generated and the previous Rx data is discarded (See Table 4, Status Register, Bits 2 and 3).

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host µController. The Rx baud rate is set by writing to the CTCSS Tx Frequency/NRZ Baud Rate Register (73$_H$/7B$_H$). The first bit received is the first bit sent to the µController.

This register is not affected by the General Reset command (01$_H$) and may adopt any random configuration at Power-Up.

"Write to NRZ Tx Data Register" – A/C 75$_H$ (7D$_H$), followed by 1 byte of Command Data.

A byte for transmission is loaded from the "C-BUS" Command Data line with this A/C. The first data-bit received via the "C-BUS" is transmitted first. This transmitter operation is **non-inverting**.

The first data-byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ Tx Data Buffer is ready for the next data-byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the Tx Sub-Audio Output placed at V$_{BIAS}$, and an interrupt generated if the next byte is not loaded within 7 bit periods. (See Table 4, Status Register, Bits 4 and 5).

This register is not affected by the General Reset command (01$_H$) and may adopt any random configuration at Power-Up.

"Write to Gain-Set Register" – A/C 76$_H$ (7E$_H$), followed by 1 byte of Command Data.

Setting				Gain Setting	
MSB					
7	**6**	**5**	**4**	**Transmitted Bit 7 First**	
0	0	0	0	These 4 Bits Must be "0"	
		3		**Pre-Emphasis Setting**	
		1		1.72dB Gain Enabled	
		0		1.72dB Gain Disabled	
2	**1**	**0**		**Tx Level Adjust Gain Setting**	
0	0	0		-2.58	dB
0	0	1		-1.72	dB
0	1	0		-0.86	dB
0	1	1		0	dB
1	0	0		+0.86	dB
1	0	1		+1.72	dB
1	1	0		+2.58	dB
1	1	1		Not Used	

Table 7 Gain-Set Register Settings

The Gain-Set Register Settings

The settings of this register control the CTCSS and NRZ signal level that is presented at the Tx Sub-Audio Output.

Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ Tx Data by increasing the gain of the data bit **before** a level change (Figure 8 below), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater than that set by Bits 0 to 2. If the Tx Sub-Audio Output level is set to +2.58dB, the pre-emphasized level will be +4.3dB.

The pre-emphasis function, will remain enabled until disabled by setting Bit 3 to a logic "0." If this function remains enabled when using the CTCSS Encoder the output signal level may be adversely affected, therefore this function should only be enabled when in the NRZ Encode mode.

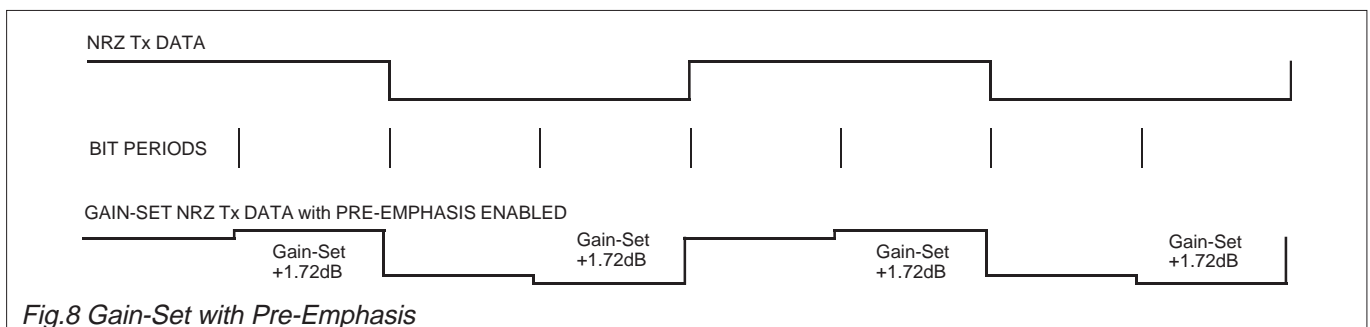This register is not affected by the General Reset command (01$_H$) and may adopt any random configuration at Power-Up.

Fig.8 Gain-Set with Pre-Emphasis

Timing Information

Timing Diagrams

Figure 9 shows the timing parameters for two-way communication between the µController and the FX805 on the "C-BUS."
Figure 10 shows, in detail, the timing relationships for "C-BUS" information transfer.

Fig.9 "C-BUS" Timing Information   NOT TO SCALE
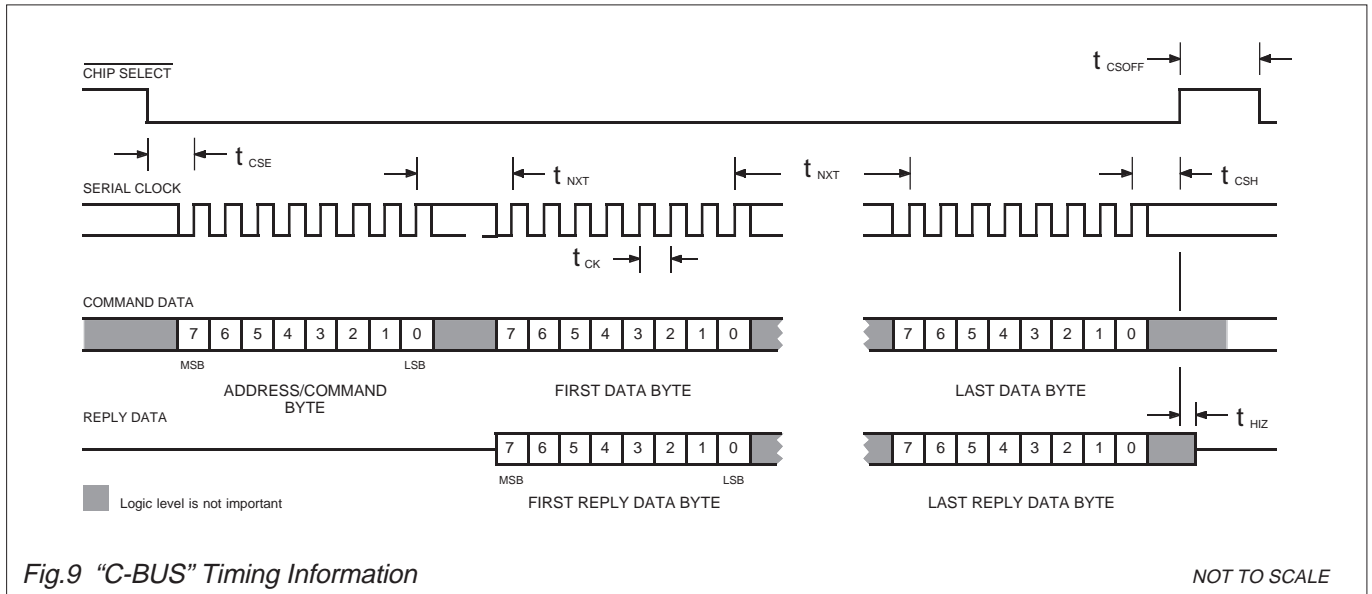
Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs
t_{CH}	500	–	–	ns
t_{CL}	500	–	–	ns
t_{CDS}	250	–	–	ns
t_{CDH}	0	–	–	ns
t_{RDS}	250	–	–	ns
t_{RDH}	50.0	–	–	ns
t_{HIZ}	–	–	2.0	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last.
Reply Data is read from the FX805 MSB (bit 7) first, LSB (bit 0) last.
(2) Data is clocked into the FX805 and into the µController on the rising Serial Clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX805 will work with either polarity Serial Clock pulses.

Fig.10 "C-BUS" Timing Relationships   NOT TO SCALE

13
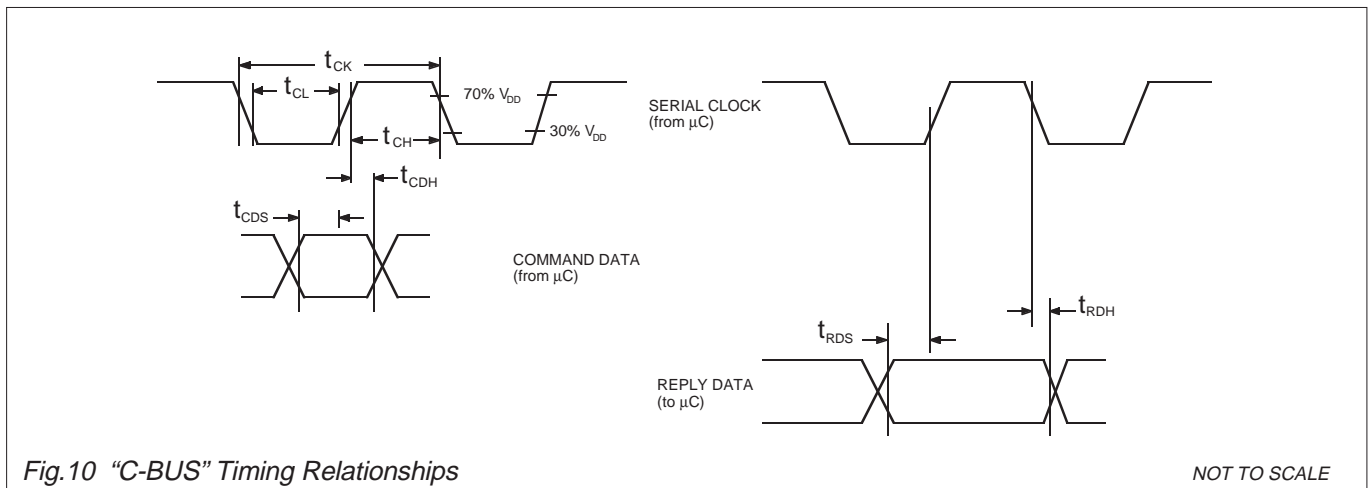
Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating temperature range: **FX805J**	-40°C to +85°C (cerdip)
FX805LG/LS	-40°C to +85°C (plastic)
Storage temperature range: **FX805J**	-55°C to +125°C (cerdip)
FX805LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_{XTAL} = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz.
Composite Signal = 308mVrms @ 1kHz + 75mVrms Noise + 31mVrms Sub-Audio Signal.
Noise Bandwidth = 5kHz Band Limited Gaussian.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	(All Functions Enabled)		–	5.0	–	mA
	(Decoders Only Enabled)		–	1.9	–	mA
	(Powersave All)		–	0.9	–	mA
Analogue Impedances						
Rx Sub-Audio Input			350	–	–	kΩ
Audio Input			350	–	–	kΩ
Audio By-Pass Switch 'On'		5	–	2.0	–	kΩ
Audio By-Pass Switch 'Off'		5	1.0	10.0	–	MΩ
Rx Amp Input (+ and -)			1.0	10.0	–	MΩ
Comparator Input (+ and -)			1. 0	10.0	–	MΩ
Rx Sub-Audio Output			–	2.0	–	kΩ
Tx Sub-Audio Output	(Encoder Enabled)	5	–	2.0	–	kΩ
	(Encoder Disabled)	5	–	500	–	kΩ
Audio Output	(Enabled)	5	–	2.0	–	kΩ
	(Disabled)	5	–	500	–	kΩ
Rx Amp and Comparator Outputs						
Large Signal			–	6.0	–	kΩ
Small Signal			–	600	–	Ω
Dynamic Values						
Digital Interface						
Input Logic "1"		1	3.5	–	–	V
Input Logic "0"		1	–	–	1.5	V
Output Logic "1"	(IOH = -120μA)	2	4.6	–	–	V
Output Logic "0"	(IOL = 360μA)	3	–	–	0.4	V
I_{OUT} Tristate (Logic "1" or "0")		3	–	–	4.0	μA
Input Capacitance		1	–	–	7.5	pF
Logic Input Current	(V_{IN} = 0 to 5.0V)	1	–	–	1.0	μA
IOX	(V_{OUT} = 5.0V)	4	–	–	4.0	μA
Overall Performance						
CTCSS – Decode						
Sensitivity	(Pure CTCSS Tone)	6	–	-26.0	–	dB
Response Time	(Composite Signal)					
100Hz to 257Hz Tone			–	–	250	ms
65Hz Tone		9	–	–	375	ms
Tone Measurement Resolution			–	0.2	–	%
Tone Measurement Accuracy			–	0.5	–	%
NOTONE Response Time	(Composite Signal)	7	–	–	250	ms
False Tone Interrupts	(Noise input only)	10	–	20.0	–	/Hr

Specification ......

| Characteristics	See Note	Min.	Typ.	Max.	Unit
CTCSS – Encode					
Frequency Range		65.0		257	Hz
Tone Frequency Resolution		–	–	0.2	%
Tone Amplitude Tolerance		-1.0	–	+1.0	dB
Rise Time (to 90%)		–	–	30.0	ms
Fall Time (to 10%)		–	–	50.0	ms
Total Harmonic Distortion		–	–	5.0	%
NRZ – Decode					
Rx Bit-Rate Sync Time		–	2	–	edges
Rx Bit Error Rate	11	–	1×10^{-3}	–	$P_{(error)}$
NRZ – Tx					
Tx Bit Rate		67.0	–	300	bits/s
Tx LPF (3dB) Bandwidth		75	–	300	Hz
Sub-Audio Tx Output Level					
CTCSS		–	0	–	dB
NRZ		–	0.871	–	V p-p
Amplitude Adjustment Range		-2.58		2.58	dB
Adjustment Step Size (7 steps)	8	–	0.86	–	dB
Sub-Audio Bandstop Filter					
Passband		300		3000	Hz
Passband Gain		–	0	–	dB
Passband Gain (w.r.t. gain at 1.0kHz)		-1.5	–	+0.5	dB
Stopband Attenuation					
at 250 Hz		–	36.0	–	dB
at 150 Hz		–	24.0	–	dB
at 100 Hz		–	18.0	–	dB
Residual Hum and Noise		–	-50.0	-46.0	dBp
Alias Frequency		–	–	62.5	kHz
Xtal/Clock Frequency (f_{XTAL})		3.9	–	4.1	MHz

Notes

1. Device control pins; Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. Reply Data and $\overline{\text{IRQ}}$ outputs.
4. Leakage current into the "Off" $\overline{\text{IRQ}}$ output.
5. See Control Register.
6. With Input gain components set as recommended in Figure 2.
7. Probability 0.97
8. See Gain-Set Register, Table 7 - Bits 0, 1, 2 and 3.
9. For $f_{CTCSS\,IN}$ of 65Hz to 100Hz, Response Time $t_R = (100/f_{TONE})$ x 250 ms.
10. Distributed across the Rx frequency band.
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.

Package Outlines

The FX805 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.
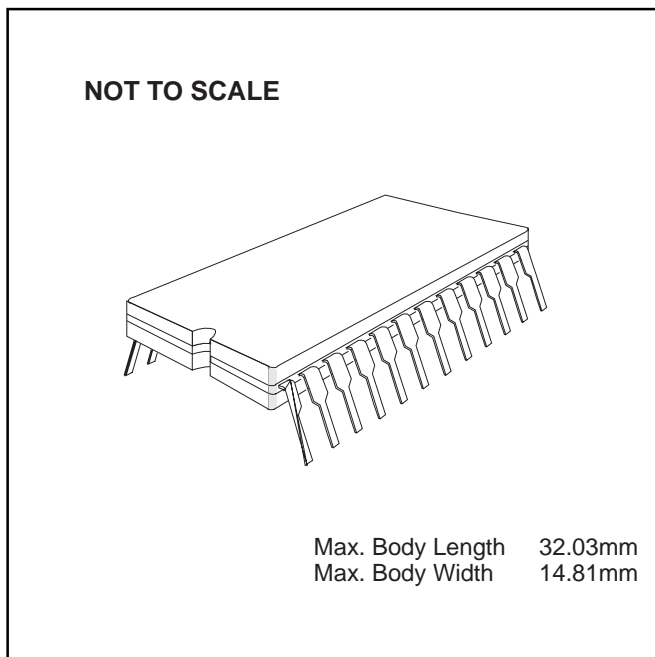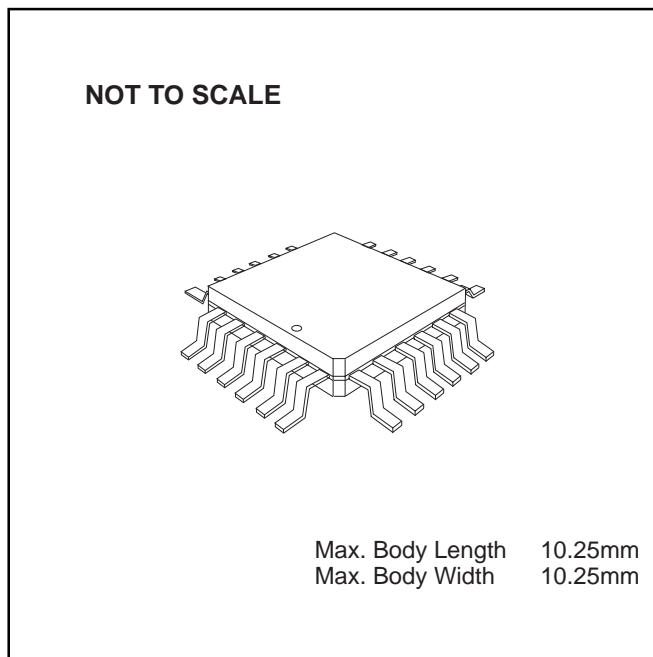
Handling Precautions

The FX805 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX805J 24-pin cerdip DIL (J4)

NOT TO SCALE

Max. Body Length   32.03mm
Max. Body Width   14.81mm

FX805LG 24-pin quad plastic encapsulated bent and cropped (L1)

NOT TO SCALE

Max. Body Length   10.25mm
Max. Body Width   10.25mm

FX805LS 24-lead plastic leaded chip carrier (L2)

NOT TO SCALE

Max. Body Length   10.40mm
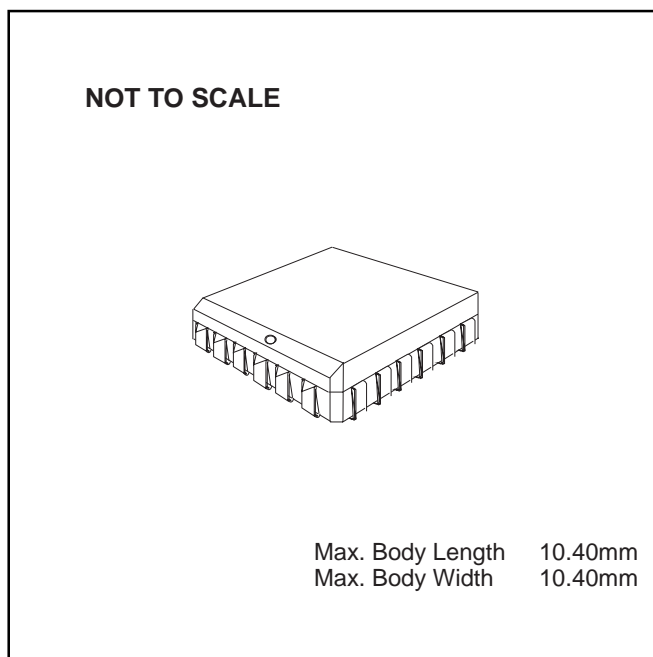Max. Body Width   10.40mm

Ordering Information

FX805J   24-pin cerdip DIL   (J4)

FX805LG   24-pin encapsulated bent and cropped   (L1)

FX805LS   24-lead plastic leaded chip carrier   (L2)

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd)*, now operate under the single title **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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D/CML (D)/1 February 2002