PRODUCT INFORMATION

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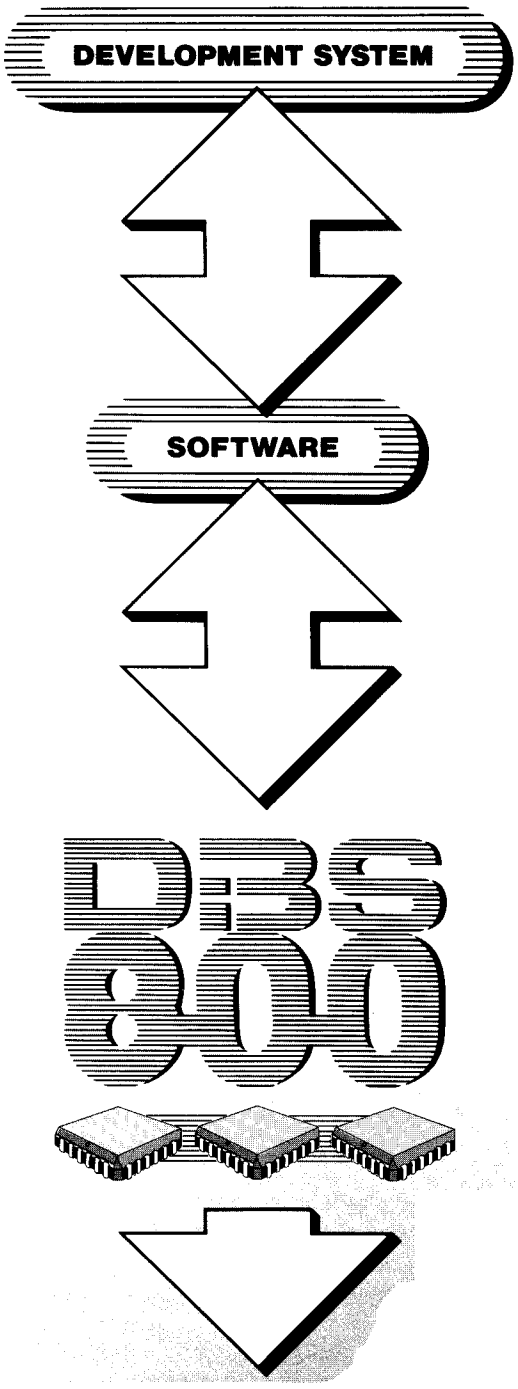


DBS 800

Technical Data Sheet

FX806 Audio Processor

Island Labs

The Digitally-integrated Baseband System, DBS 800, is a combination of Application Specific Integrated Circuits, Development PCBs and Control Software.
Designed specifically for use within Mobile and Trunked Radio Equipment, DBS 800 provides Audio Processing, System Signalling, Data Communications and Advanced Voice Management facilities. DBS 800 satisfies all current Mobile Radio requirements and ensures that future upgrades are catered for.
The FX806 integrated circuit provides all the Audio processing and signal conditioning required by the DBS 800.

FX806
AUDIO PROCESSOR

Island Labs

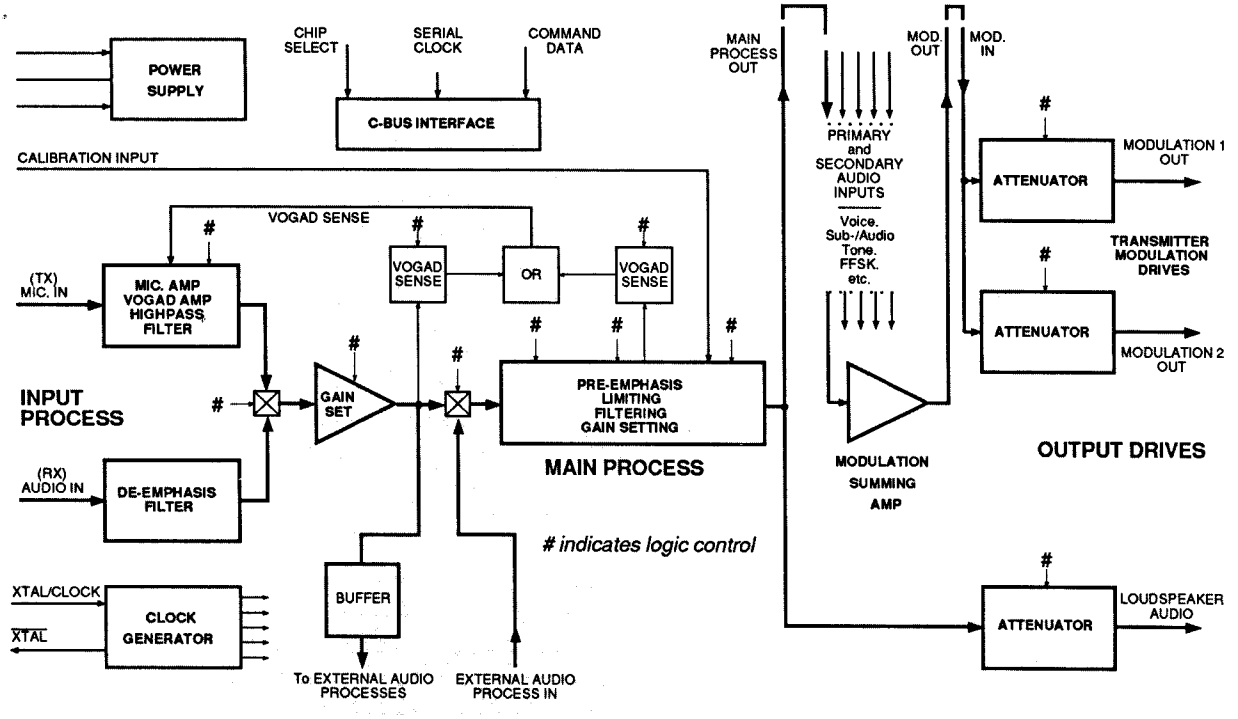


Fig.1 FX806 Audio Processor

Description

The FX806 is a PMR Audio Processor intended primarily to operate as the "Audio Terminal" of Radio Systems using the DBS 800 Digitally-Integrated Baseband System.

The FX806 is a half-duplex device whose signal paths and level setting elements are configured and adjusted by digital information sent from the Radio µController using "C-BUS" hardware and software protocol.

The signal path of the FX806 can be viewed as 3 sections:

- **Input Process**
  Selectable transmit or receive input paths. Transmit voice signals pass through microphone pre-amplifier, voltage controlled gain (VOGAD) and highpass filter stages. Received audio is de-emphasised.
  This initial audio, after in-line gain adjustment, is available for switching to either external audio processes (such as scrambling) or internally to the Main Process stages.
- **Main Process**
  Conditioning for Input or External Process signals with pre-emphasis, high and lowpass switched capacitor filters and a transmitter deviation limiter.
- **Summation and Output Drives**
  Main "voice audio" for transmission is combined with signalling and data from other DBS 800 microcircuits, to provide the composite (in and outband) signal for the digitally adjustable Transmitter Modulation Drives.
  Received audio is level (volume) adjusted for output to loudspeaker circuitry.

Figure 5 shows a complete functional block diagram of the FX806.

Signal-level stability and therefore output accuracy, of the FX806 is maintained by a voltage-controlled gain system using selectable signal-level detectors.

Signal levels can be dynamically controlled to provide 'dynamic-compensation' for such factors as temperature drift, VCO non-linearity, etc.

FX806 audio output stages can be completely disabled or the whole microcircuit placed into a "Powersave" mode, leaving only clock and "C-BUS" circuitry active.

The FX806 is a low-power, 5-volt CMOS integrated circuit and is available in 24-pin DIL cerdip and 24-pin/ lead plastic SMD packages.

FX806 J/LG/LS	
1	**Xtal:** The output of the on-chip clock oscillator. External components are required at this output when a Xtal is employed. See Figure 2, INSET 2.
2	**Xtal/clock**: The input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, INSET 2. This clock provides timing for on-chip elements, filters etc.
3	**Serial Clock:** The "C-BUS," serial data loading clock input. This clock, produced by the µController, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams and System Support Document (Document 2).
4	**Command Data:** The "C-BUS," serial data input from the µController. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1, 2, 3, 4 and 5. See Timing diagrams and System Support Document (Document 2).
5	**Chip Select ($\overline{CS}$):** The "C-BUS," data loading control function. This input is provided by the µController. Command Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing diagrams and System Support Document (Document 2).
6	**VOGAD Out:** The output of the selected VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin.
7	**Rx Audio In:** The audio input to the FX806 from the radio receiver's demodulator circuits. This input, which requires to be a.c. coupled with capacitor C_{12}, is selected by a Control Command bit.
8	**VOGAD In:** The gain control signal from the selected VOGAD sensor to the Input Process Voltage Controlled Amplifier. The required sensor is selected via a Mode Command. The choice of two sensors enables gain control from either the Input Process or an External Process. External attack and decay setting components should be applied as recommended in Figures 2 and 3.
9	**V_{BIAS}:** The output of the on-chip analogue circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by a capacitor C_{10}, See Figure 2.
10	**Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1.
11	**Mic In (–):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2, INSET 1.
12	**V_{SS}:** Negative supply rail (GND).

Pin Number Function

FX806 J/LG/LS	
13	**Mic Out:** The output of the microphone Op-Amp, used with the Mic In (–) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at V_{SS}.
14	**Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires to be a.c. coupled with a capacitor, C_{13}, is selected by a Mode Command bit.
15	**External Audio Process:** The buffered output of the Input Processing stage. For further external audio processing prior to re-introduction at the Processed Audio In pin.
16	**Calibration Input:** A unique audio input, intended to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the FX803 Audio Tone Processor can be entered on this line. The audio input to this pin requires to be externally biased and is selected via a Mode Command bit.
17	**Main Process Out:** The output of the Main Process stage. This output is summed with additional system inputs as required (Audio, Sub-Audio Signalling, FFSK – See Document 1, System Overview) in the on-chip Modulation Summing Amplifier. External components as shown in Figure 2 should be used as required.
18	**Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals, with gain/attenuation setting as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In.
19	**Sum Out:**
20	**Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives.
21	**Audio Output:** The processed audio signal output intended as a received audio (volume) output. Though normally used in the Rx mode, operation in Tx is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	**Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO), from the composite audio summing stage.
23	**Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator, from the composite audio summing stage. **NOTE:** These VCO output attenuators are individually adjustable using the Modulator Level command. During Powersave these outputs are placed at V_{SS}.
24	V_{DD}: Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the Audio Processor are dependant upon this supply.

External Components

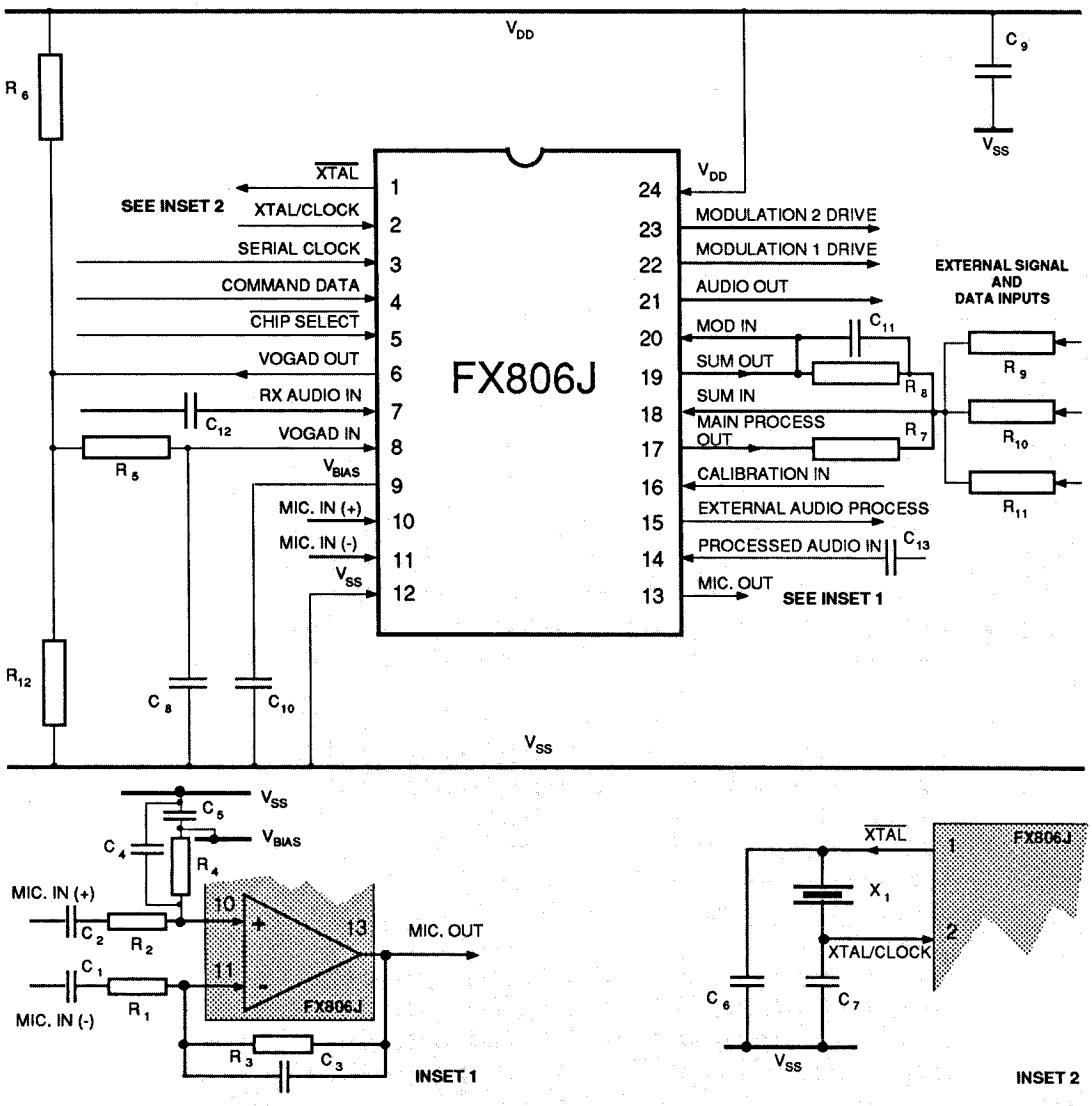


Fig.2 Recommended External Components

Component		Value						
R_1	=	10.0kΩ	R_{10}	=	100kΩ	C_7	=	5 – 65pF
R_2		10.0kΩ	R_{11}		100kΩ	C_8		1.0µF
R_3		20.0kΩ	R_{12}		2.2MΩ	C_9		1.0µF
R_4		20.0kΩ	C_1		470nF	C_{10}		1.0µF
R_5		10.0kΩ	C_2		470nF	C_{11}		22pF
R_6		2.2MΩ	C_3		270pF	C_{12}		100nF
R_7		100kΩ	C_4		270pF	C_{13}		10.0nF
R_8		100kΩ	C_5		0.1µF	X_{13}		4.0MHz
R_9		100kΩ	C_6		33pF			

Tolerance: R = ±10%. C = ± 20%

Notes

Input Op-Amp gain/attenuation components (voltage gain = 6.0dB) are shown (INSET 1) in a differential configuration to demonstrate the versatility of this input. Components for a single (+ or -) input may be employed.

Resistor values R_7 to R_{11} (summation components) are dependant upon application and configuration requirements.

Xtal circuit capacitors C_6 (C_D) and C_7 (C_G) shown (INSET 2) are recommended in accordance with *CML Application Note D/XT/1 April 1986.* Circuit drive and drain resistors are incorporated on-chip.

The Gain Control System

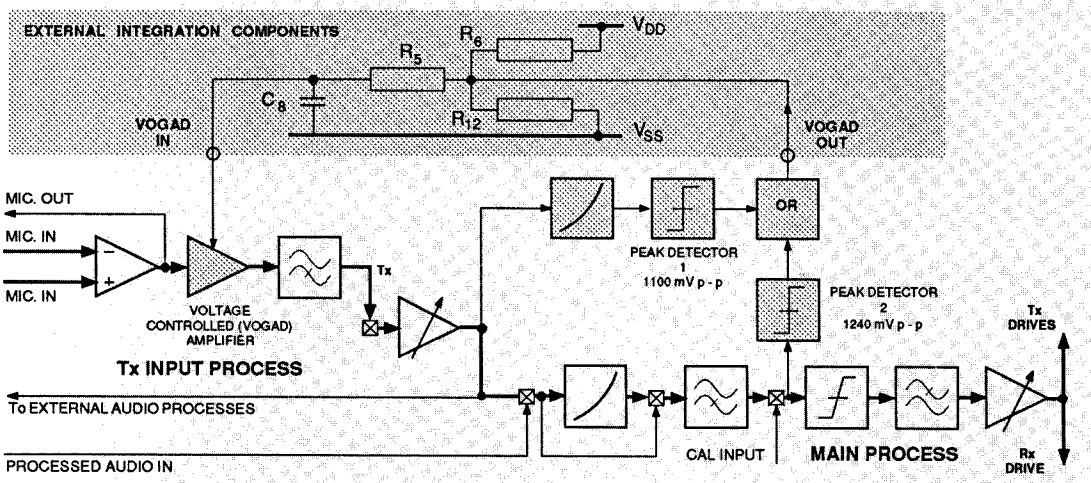


Fig.3 "VOGAD" Sensors and Timing Components – (part of Fig.5)

The overall Gain Control system of the FX806 consists of 2 selectable signal peak detectors whose output is fed via external integrating components to adjust the gain of the Voltage Controlled Amplifier positioned in the Tx Input Process Path. The transmit input signal is presented to Peak Detector 1 or 2. The Peak Detectors are enabled individually by a Mode command. When the input signal exceeds the peak-to-peak threshold of the detector a 5-volt level is produced at the VOGAD Out pin, this level remains for as long as the signal exceeds the threshold.

The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. As can be seen from Figures 3 and 5, Peak Detector 1 allows control of the audio level to the external audio process and Peak Detector 2 allows control of transmit deviation levels.
VOGAD attack and decay times are set using the external components shown in Figures 2 and 3, and are calculated as described below.

VOGAD Components Calculations – Figures 2 and 5

Provided R_5 >>1.0kΩ and $R_6 = R_{12}$ >>R_5

Then:

Attack Time (T_A) = $R_5 \times C_8$

Decay Time (T_D) = $\frac{R_6 \times C_8}{2}$

Suggested Calibration Methods

To effectively null all internal microcircuit tolerances, the following initial calibration routine is suggested:

Tx Calibration : From Mic. In to Modulator Drives Out

Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

(1) Mic. In = 250mVrms at 1kHz; Set Process Gain Amp for output of 1440mV p - p (100% deviation).
(2) With Process Gain Amp set as (1); Mic In = 25mVrms at 1kHz, set Input Level Amp for output level of 308 mVrms (60% deviation).

Rx Calibration: From Rx Audio In to Audio Out

Set Audio Output Drive to 0dB (Volume Set).
Leave Process Gain Amp set as In (1) (above).
(3) With Rx Audio In level of between 154mVrms and 308mVrms (see Specification page), at 1kHz, set the Input Level Amp for an output level of 308mVrms.

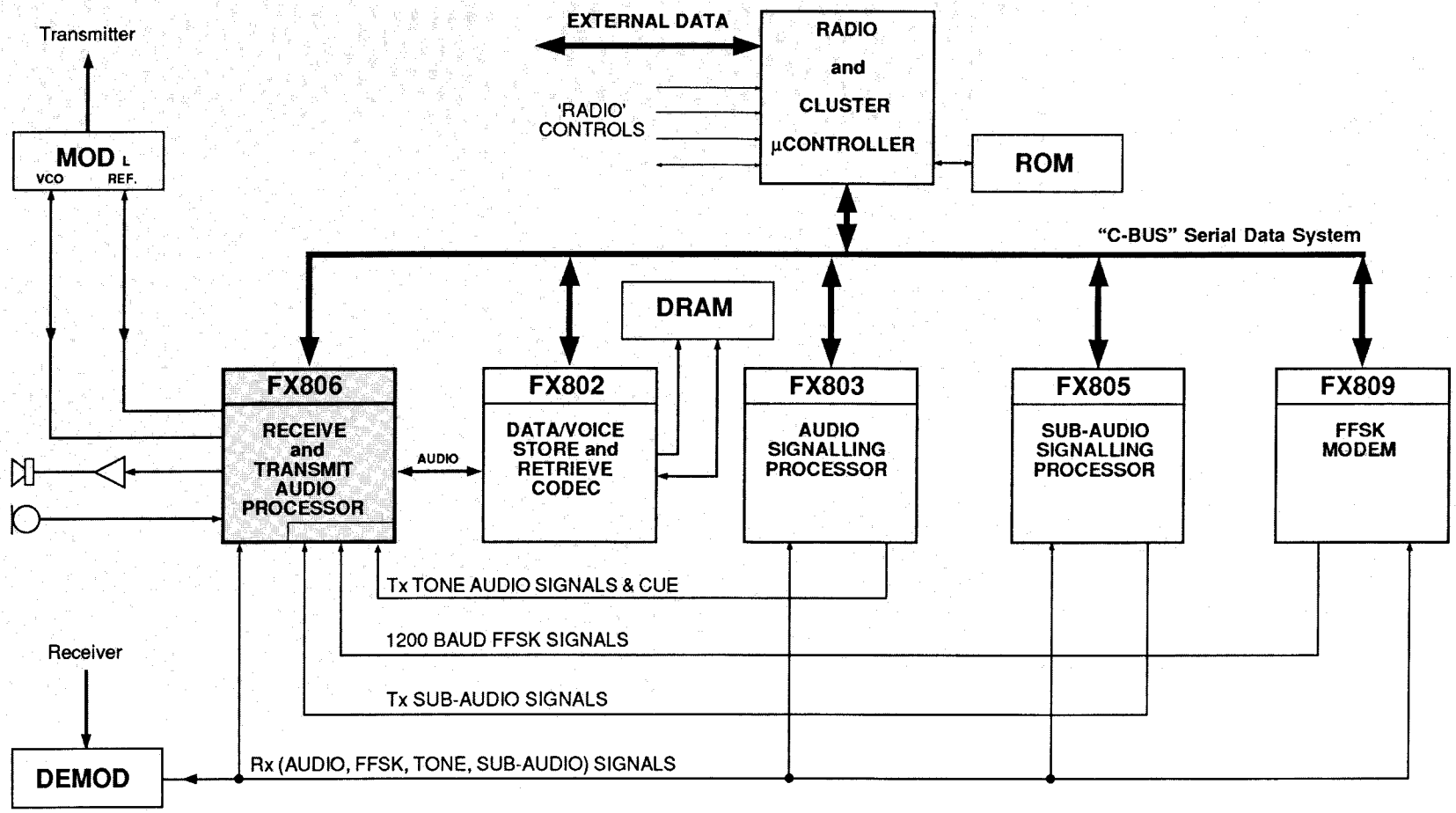


Fig.4 FX806 Interfaced With Other DBS 800 Elements

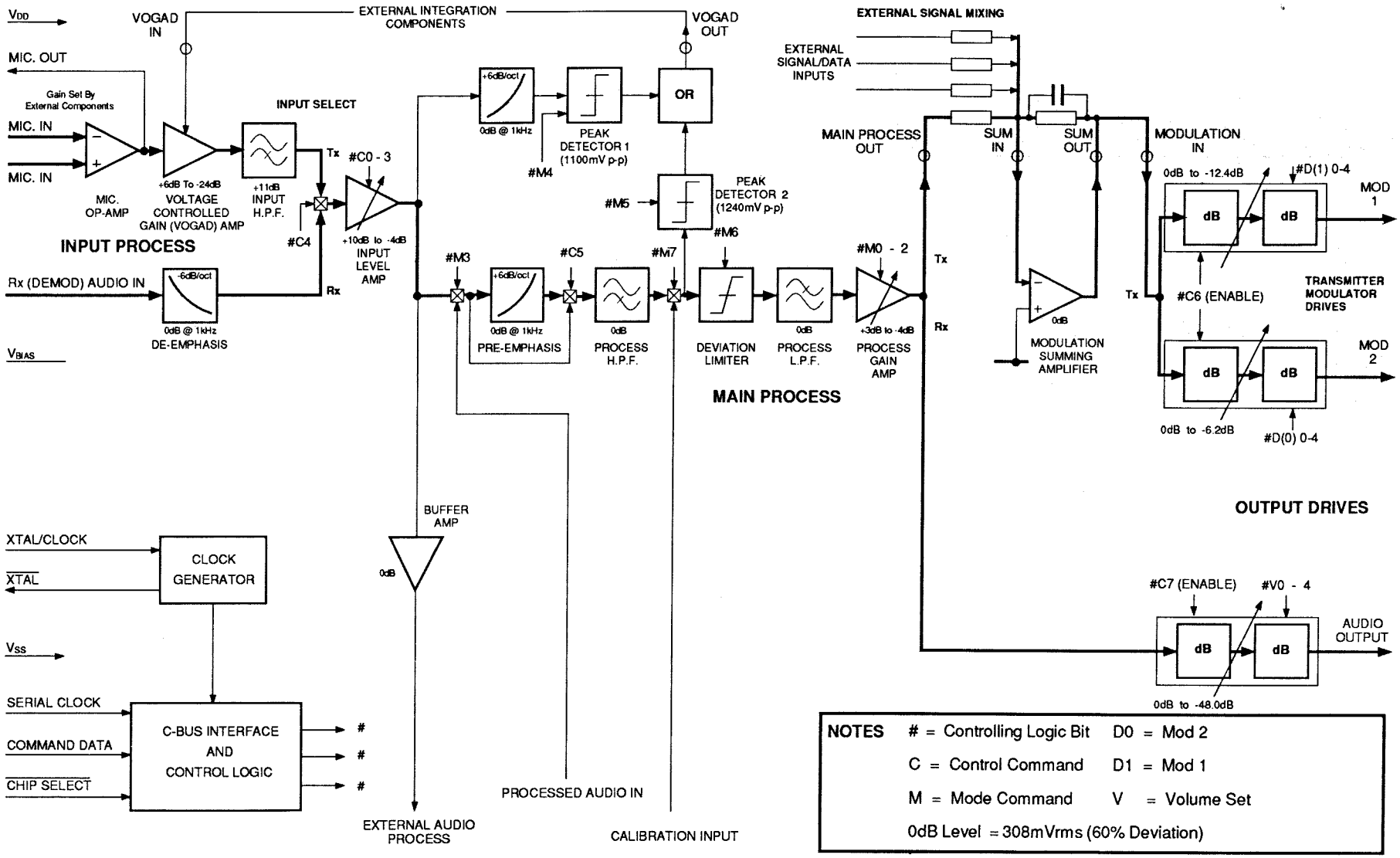


Fig.5 PLMR Audio Processor – Facilities

Controlling Protocol

Control of the functions and levels within the FX806 PLMR Audio Processor is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX806. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Control Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Mode Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Mod. Levels Set	12	0 0 0 1 0 0 1 0	+	2 bytes	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In "C-BUS" protocol the FX806 is allocated Address/Command (A/C) values 10_H to 13_H. "C-BUS" Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5 (Main Block Diagram). Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the "C-BUS" interface recognises the first byte after Chip Select (logic "0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) will be required. This command is provided to "reset" all devices on the "C-BUS" and has the following effect on the FX806.

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

Control Command

(Preceded by A/C 10_H)

Setting	Control Bits
MSB Bit 7	***Transmitted First***
	Audio Output (Rx)
0	Disabled
1	Enabled
6	**Modulation Drives**
0	Disabled
1	Enabled
5	**Pre-Emphasis Select**
0	By-Pass
1	Enabled
4	**Input Select**
0	Rx Audio In
1	Mic. In
3 2 1 0	**Input Level Set**
0 0 0 0	Input Amp Disabled
0 0 0 1	-4.0dB
0 0 1 0	-3.0dB
0 0 1 1	-2.0dB
0 1 0 0	-1.0dB
0 1 0 1	0dB
0 1 1 0	1.0dB
0 1 1 1	2.0dB
1 0 0 0	3.0dB
1 0 0 1	4.0dB
1 0 1 0	5.0dB
1 0 1 1	6.0dB
1 1 0 0	7.0dB
1 1 0 1	8.0dB
1 1 1 0	9.0dB
1 1 1 1	10.0dB

Table 2 Control Commands

Mode Command

(Preceded by A/C 11_H)

Setting	Mode Bits
MSB Bit 7	***Transmitted First***
	Drive Source
0	Signals
1	Calibration
6	**Deviation Limiter**
0	Disabled
1	Enabled
5	**Peak Detect 2**
0	Disabled
1	Enabled
4	**Peak Detect 1**
0	Disabled
1	Enabled
3	**Input Signal Select**
0	Primary Inputs (Mic., Rx)
1	External Process
2 1 0	**Process Level Set**
0 0 0	-4.0dB
0 0 1	-3.0dB
0 1 0	-2.0dB
0 1 1	1.0dB
1 0 0	0dB
1 0 1	1.0dB
1 1 0	2.0dB
1 1 1	3.0dB

Table 3 Mode Commands

Modulator Levels

(Preceded by A/C12$_H$)

Setting					Modulator Drives
Byte 1					***First byte for transmission***
MSB					
7		***6***		***5***	
0		0		0	Must be "0"
4	***3***	***2***	***1***	***0***	**Mod. 1** Attenuation
0	0	0	0	0	12.4dB
0	0	0	0	1	12.0dB
0	0	0	1	0	11.6dB
0	0	0	1	1	11.2dB
0	0	1	0	0	10.8dB
0	0	1	0	1	10.4dB
0	0	1	1	0	10.0dB
0	0	1	1	1	9.6dB
0	1	0	0	0	9.2dB
0	1	0	0	1	8.8dB
0	1	0	1	0	8.4dB
0	1	0	1	1	8.0dB
0	1	1	0	0	7.6dB
0	1	1	0	1	7.2dB
0	1	1	1	0	6.8dB
0	1	1	1	1	6.4dB
1	0	0	0	0	6.0dB
1	0	0	0	1	5.6dB
1	0	0	1	0	5.2dB
1	0	0	1	1	4.8dB
1	0	1	0	0	4.4dB
1	0	1	0	1	4.0dB
1	0	1	1	0	3.6dB
1	0	1	1	1	3.2dB
1	1	0	0	0	2.8dB
1	1	0	0	1	2.4dB
1	1	0	1	0	2.0dB
1	1	0	1	1	1.6dB
1	1	1	0	0	1.2dB
1	1	1	0	1	0.8dB
1	1	1	1	0	0.4dB
1	1	1	1	1	0dB
Byte 0					***Last byte for transmission***
MSB					
7		***6***		***5***	
0		0		0	Must be "0"
4	***3***	***2***	***1***	***0***	**Mod. 2** Attenuation
0	0	0	0	0	6.2dB
0	0	0	0	1	6.0dB
0	0	0	1	0	5.8dB
0	0	0	1	1	5.6dB
0	0	1	0	0	5.4dB
0	0	1	0	1	5.2dB
0	0	1	1	0	5.0dB
0	0	1	1	1	4.8dB
0	1	0	0	0	4.6dB
0	1	0	0	1	4.4dB
0	1	0	1	0	4.2dB
0	1	0	1	1	4.0dB
0	1	1	0	0	3.8dB
0	1	1	0	1	3.6dB
0	1	1	1	0	3.4dB
0	1	1	1	1	3.2dB
1	0	0	0	0	3.0dB
1	0	0	0	1	2.8dB
1	0	0	1	0	2.6dB
1	0	0	1	1	2.4dB
1	0	1	0	0	2.2dB
1	0	1	0	1	2.0dB
1	0	1	1	0	1.8dB
1	0	1	1	1	1.6dB
1	1	0	0	0	1.4dB
1	1	0	0	1	1.2dB
1	1	0	1	0	1.0dB
1	1	0	1	1	0.8dB
1	1	1	0	0	0.6dB
1	1	1	0	1	0.4dB
1	1	1	1	0	0.2dB
1	1	1	1	1	0dB

Table 4 Modulator Drive Levels

Volume Set

(Preceded by A/C13$_H$)

Setting					Volume Set
MSB					***Transmitted First***
7		***6***			
0		0			Must be "0"
		5			**Powersave**
		0			Chip Enabled
		1			Powersaved
4	***3***	***2***	***1***	***0***	**Volume Set** Attenuation
0	0	0	0	0	Off
0	0	0	0	1	48.0dB
0	0	0	1	0	46.4dB
0	0	0	1	1	44.8dB
0	0	1	0	0	43.2dB
0	0	1	0	1	41.6dB
0	0	1	1	0	40.0dB
0	0	1	1	1	38.4dB
0	1	0	0	0	36.8dB
0	1	0	0	1	35.2dB
0	1	0	1	0	33.6dB
0	1	0	1	1	32.0dB
0	1	1	0	0	30.4dB
0	1	1	0	1	28.8dB
0	1	1	1	0	27.2dB
0	1	1	1	1	25.6dB
1	0	0	0	0	24.0dB
1	0	0	0	1	22.4dB
1	0	0	1	0	20.8dB
1	0	0	1	1	19.2dB
1	0	1	0	0	17.6dB
1	0	1	0	1	16.0dB
1	0	1	1	0	14.4dB
1	0	1	1	1	12.8dB
1	1	0	0	0	11.2dB
1	1	0	0	1	9.6dB
1	1	0	1	0	8.0dB
1	1	0	1	1	6.4dB
1	1	1	0	0	4.8dB
1	1	1	0	1	3.2dB
1	1	1	1	0	1.6dB
1	1	1	1	1	0dB

Table 5 Volume Set

Command Loading Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6 (Timing).

The **Powersave** function is instigated by bit 5 of the Volume Set Command (Table 5).

During Powersave, all internal elements except the Clock Generator and "C-BUS" Interface are off, with the Mic Op-Amp and Output Drive stage outputs connected to V_{SS}.

Modulator Drives are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each required adjustment.

$\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX806J**	-40°C to +85°C (cerdip)
	FX806LG/LS	-40°C to +85°C (plastic)
Storage temperature range:	**FX806J**	-55°C to +125°C (cerdip)
	FX806LG/LS	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Audio Level 0dB ref: = 308mVrms @ 1kHz *(60% deviation, FM).*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All Elements Enabled)		–	6.0	–	mA
(Maximum Powersave)		–	0.6	–	mA
"C-BUS" Interface					
Input Logic "1"		3.5	–	–	V
Input Logic "0"		–	–	1.5	V
Input Leakage Current (logic "1 or 0")		-1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
Dynamic Values					
Overall Performance					
Microphone Input	4, 5	–	25.0	–	mVrms
Rx Audio In	6, 5	154	–	308	mVrms
Output Drive Levels					
For 60% Deviation	5, 7	291	308	326	mVrms
For 100% Deviation	5, 7, 8	–	1,440	–	mV p - p
Passband Frequencies	1	297	–	3000	Hz
Passband Ripple	2	-2.0		0.5	dB
Stopband Attenuation	1, 3				
f = 150Hz		10.0	12.0	–	dB
f = 3400Hz		–	2.0	–	dB
f = 6000Hz		30.0	36.0	–	dB
f = 8000Hz to 20,000Hz		–	60.0	–	dB
Signal Path Noise					
Rx		–	-60.0	–	dBp
Rx	10	–	-55.0	–	dB
Tx		–	-50.0	–	dBp
Tx	10	–	-45.0	–	dB
Distortion		–	1.0	–	%
Circuit Elements – Figure 5					
Mic Amp or Mod Summation Amp					
Open Loop Gain		–	50.0	–	dB
Bandwidth		20.0	–	–	kHz
Input Impedance		10.0	–	–	MΩ
Output Impedance (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
De-emphasis					
Slope		–	-6.0	–	dB/oct.
Gain (at 1.0kHz)		–	0	–	dB
Input Impedance		–	1.0	–	MΩ
Voltage Controlled Gain Amp					
Gain (Non-Compressing)	5	–	6.0	–	dB
(Full Compression)		–	-24.0	–	dB
VOGAD In Input Impedance		–	10.0	–	MΩ

Characteristics	See Note	Min.	Typ.	Max.	Unit
VOGAD Peak Detectors					
Output Impedance - Logic "1" (Compress)		–	1.0	–	kΩ
- Logic "0"		–	10.0	–	MΩ
Peak Detector 1 Threshold	11	–	1,100	–	mV p - p
Peak Detector 2 Threshold	11	–	1,240	–	mV p - p
Input Highpass Filter					
Gain (at 1.0kHz)		10.0	11.0	12.0	dB
Input Level Amp					
Gain Range		-4.0		10.0	dB
Overall Tolerance		-1.0	–	1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope		–	6.0	–	dB/oct.
Gain (at 1.0kHz)		–	0	–	dB
Process Highpass Filter					
Gain (at 1.0kHz)		-1.0	0	1.0	dB
Deviation Limiter					
Threshold		411	436	461	mVrms
Gain		-0.5	–	0.5	dB
Process Lowpass Filter					
Gain (at 1.0kHz)		-1.0	0	1.0	dB
Process Gain Amp					
Gain Range		-4.0		3.0	dB
Overall Tolerance		-0.5	–	0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance		–	600	–	Ω
Transmitter Modulator Drives					
Input Impedance		–	15.0	–	kΩ
Mod.1 Attenuator					
Attenuation Range		0		12.4	dB
Overall Tolerance		-1.0	–	1.0	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance		–	600	–	Ω
Mod.2 Attenuator					
Attenuation Range		0		6.2	dB
Overall Tolerance		-0.5	–	0.5	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance		–	600	–	Ω
Audio Output Attenuator					
Attenuation Range		0		48.0	dB
Overall Tolerance		-0.5	–	0.5	dB
Step Size		1.1	1.6	2.1	dB
Output Impedance		–	600	–	Ω
Miscellaneous Impedances					
Processed Audio Input		–	1.0	–	MΩ
Calibration Input		–	40.0	–	MΩ
External Process Out		–	100	–	Ω

Notes

1. Between Mic. or Rx inputs to Modulator or Audio outputs.
2. The deviation from the ideal overall response that includes the pre- or de-emphasis slope.
3. Excluding the effect of the pre- or de-emphasis slope.
4. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
5. With Output Drives set to 0dB and the system calibrated, as described in the Application notes.
6. Input level range for 0dB output, by adjustment of the Input Level Amp.
7. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
8. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
9. Using external components recommended in Figure 2.
10. In a 30kHz bandwidth.
11. Using Pre-emphasis in the Tx path.

Command Loading and Timing

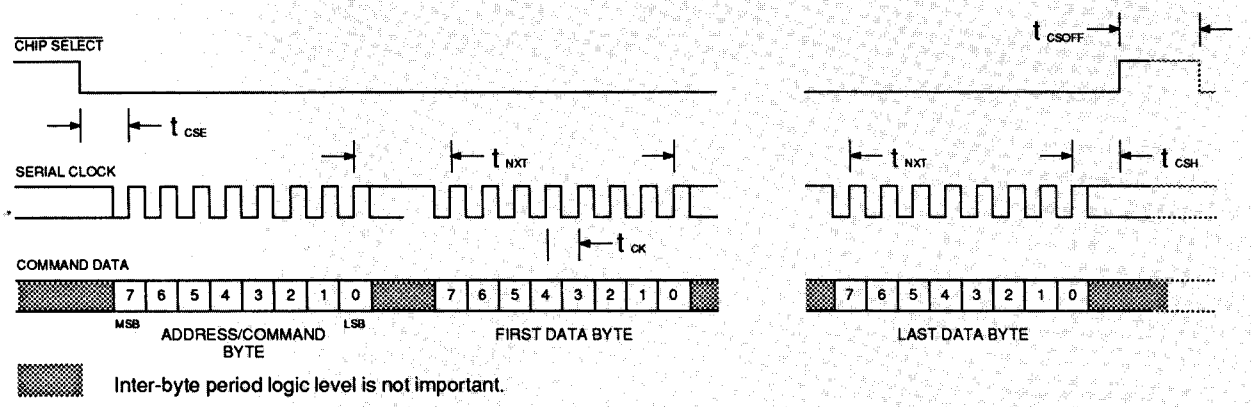


Fig.6 "C-BUS" Timing Information

Parameter	Min.	Typ.	Max.	Unit
t_{CSE}	2.0	–	–	µs
t_{CSH}	4.0	–	–	µs
t_{CSOFF}	2.0	–	–	µs
t_{NXT}	4.0	–	–	µs
t_{CK}	2.0	–	–	µs

Notes

(1) Command Data is transmitted to the peripheral MSB (bit7) first, LSB (bit0) last.
(2) Data is clocked into the peripheral on the rising clock edge.
(3) Loaded data instructions are acted upon at the end of each individual, loaded byte.
(4) To allow for differing µController serial interface formats, the FX806 will work with either polarity Serial Clock pulses.

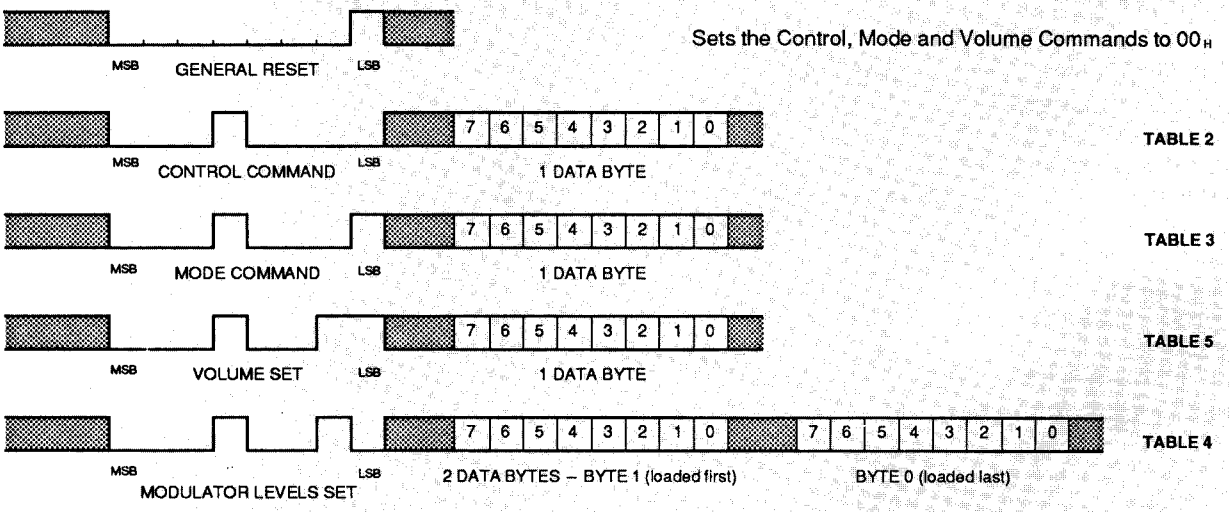


Fig.7 Examples of "Command Data" Configurations

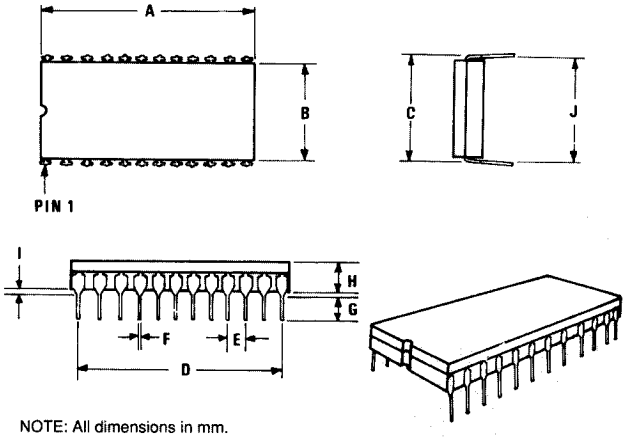
To assist in rapid setting, the "quick-reference" guide below should be used with Figure 5.

Control	**A/C = 10_H**
Bit 7	Audio Out (Rx) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Select
4	Input Select (Rx/Tx)
3 – 0	Input Level Set (-4dB to 10dB)
Mode	**A/C = 11_H**
Bit 7	Drive Source
6	Deviation Limiter Enable
5	Peak Detect 2 Enable
4	Peak Detect 1 Enable
3	Input Signal Select
2 – 0	Process Level Set (-4dB to 3dB)

Modulator Levels	**A/C = 12_H**
Byte 1	
Bit 7 – 5	"0"
4 – 0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7 – 5	"0"
4 – 0	Mod 2 Attenuation (0 to 6.2dB)
Volume Set	**A/C = 13_H**
Bit 7 – 6	"0"
5	Powersave
4 – 0	Volume Set Attenuation (0 to 48dB)

Table 6 "Quick-Reference" to Command Allocations

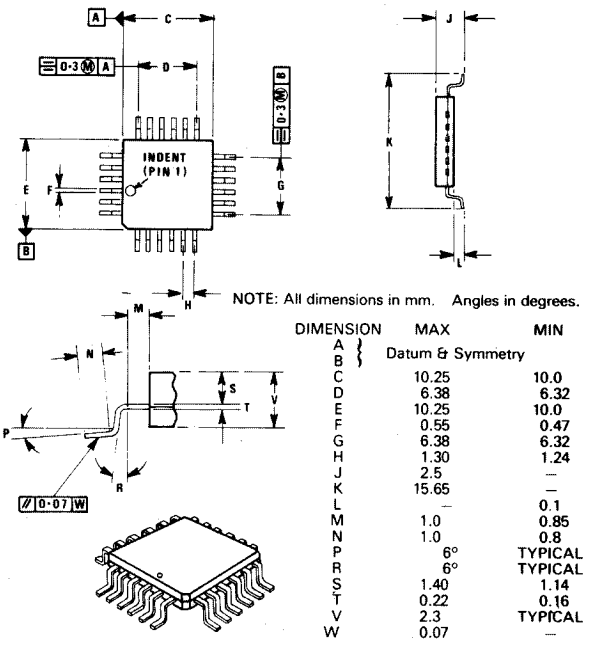
The FX806J, the dual-in-line package is shown in Figure 8. The 'LG' version is shown in Figure 9 and the 'LS' version in Figure 10.
To allow complete identification, the 'LG' and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).



NOTE: All dimensions in mm.

DIMENSION	MAX.	MIN.	DIMENSION	MAX.	MIN.
A	32.03	31.50	F	0.46	TYPICAL
B	14.81	13.06	G	4.30	4.10
C	15.61	15.14	H	4.35	3.99
D	28.04	27.84	I	1.40	TYPICAL
E	2.54	TYPICAL	J	18.20	16.54

The FX806 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	–
K	15.65	–
L	–	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	–

Ordering Information

FX806J	24-pin cerdip DIL
FX806LG	24-pin quad plastic encapsulated bent and cropped
FX806LS	24-lead plastic leaded chip carrier

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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