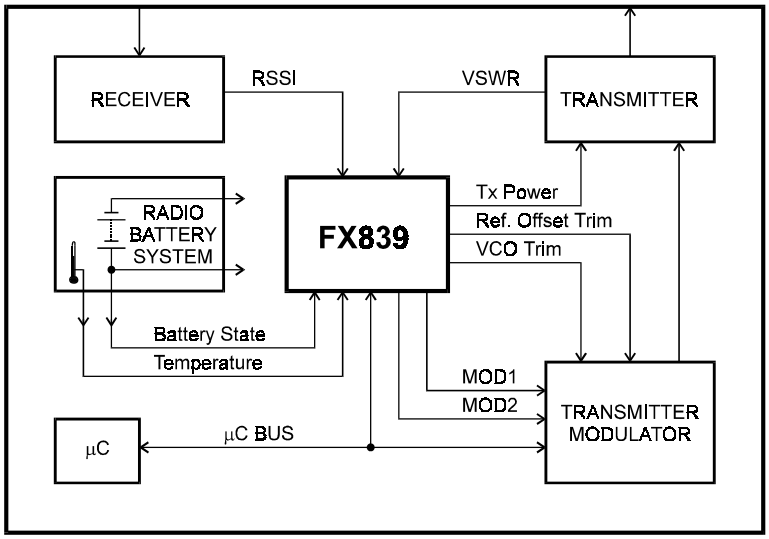
# CML Semiconductor Products

## Analogue Control Interface FX839

D/839/4 September 1997
Advance Information

### 1.0 Features

- **Three DACs 8 or 10-Bit Resolution**
- **Custom IRQ Generator with Variable 8-Bit Reference Settings**
- **Two Variable Attenuators**
- **Low Power (3.0V Operation)**
- **Multiplexed 4 Input ADC 10-Bit Resolution**
- **Scalable ADC Clock Frequencies from Xtal/Clock**
- **Serial Interface to Host µC**
- **24-Pin SSOP Package**




Island Labs

### 1.1 Brief Description

This product comprises a selection of independent functional blocks vital to modern microcomputer controlled radio-frequency communications equipment. Examples of possible uses are as follows:

- The four-way multiplexed ADC with magnitude comparator may be used for monitoring RSSI, battery voltage, temperatures, reflected signals or error voltages.
- The three DACs may be used to adjust VCOs, reference oscillators, power output, bias current or IF gain.
- The two variable attenuators may be used to adjust deviation, modulation depth or baseband gain.

The FX839 is controlled via the standard serial 'C-BUS'. This is complementary to, and compatible with, many standard microcomputers and other baseband processing blocks.

**CONTENTS**



**Note:** As this product is still in development, it is likely that a number of changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues. Information in this data sheet should not be relied upon for final product design.

## 1.2 Block Diagram

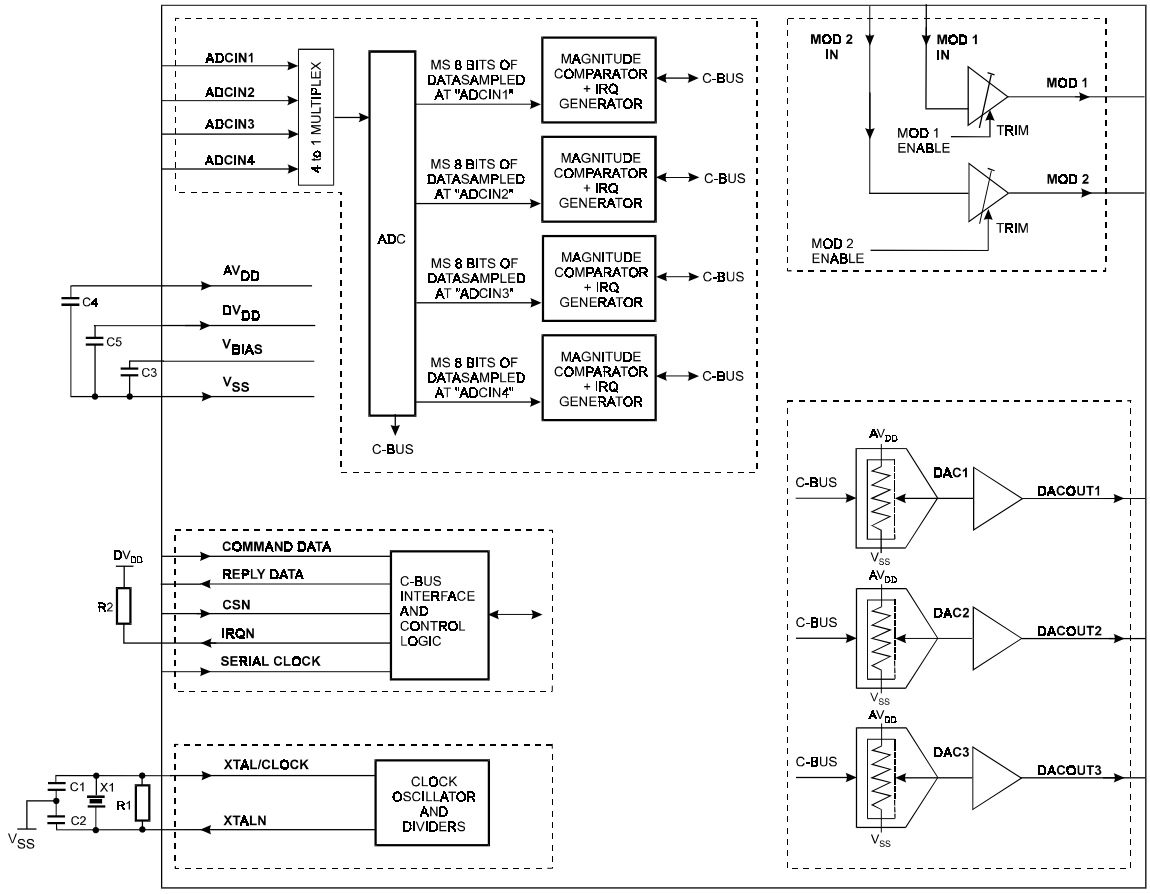



**Figure 1: Block Diagram**

## 1.3 Signal List

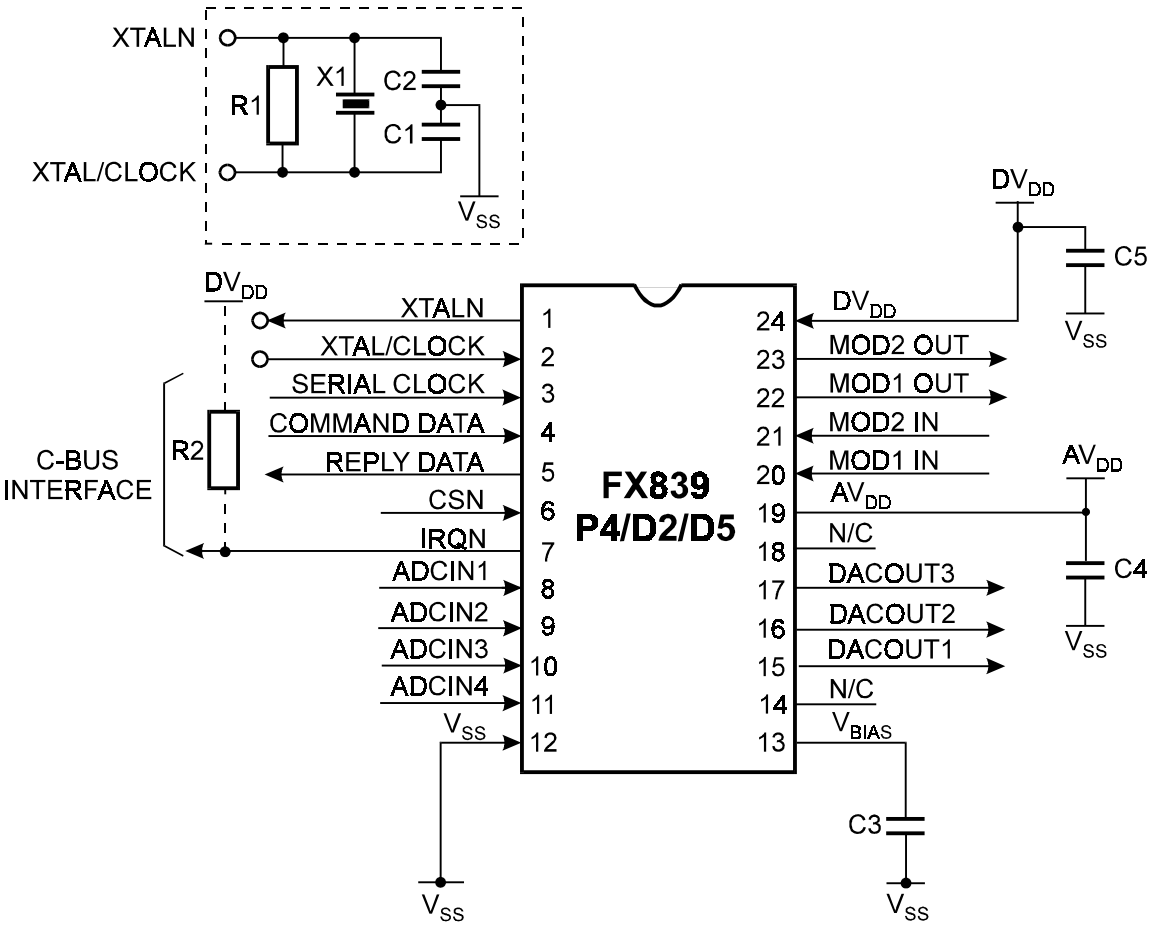
| Package P4/D2/D5 | Signal | | Description |
|---|---|---|---|
| **Pin No.** | **Name** | **Type** | |
| 1 | XTALN | O/P | The inverter output of the on-chip oscillator. |
| 2 | XTAL/CLOCK | I/P | The input to the on-chip oscillator, for external Xtal circuit or clock. |
| 3 | SERIAL CLOCK | I/P | The 'C-BUS' serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See 'C-BUS' Timing Diagram (Figure 4). |
| 4 | COMMAND DATA | I/P | The 'C-BUS' serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronised to the SERIAL CLOCK. See 'C-BUS' Timing Diagram (Figure 4). |
| 5 | REPLY DATA | O/P | The 'C-BUS' serial data output to the µController. The transmission of REPLY DATA bytes is synchronised to the SERIAL CLOCK under the control of the CSN input. This 3-state output is held at high impedance when not sending data to the µController. See 'C-BUS' Timing Diagram (Figure 4). |
| 6 | CSN | I/P | The 'C-BUS' data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the CSN signal. See 'C-BUS' Timing Diagram (Figure 4). |
| 7 | IRQN | O/P | This output indicates an interrupt condition to the µController by going to a logic '0'. This is a 'wire-ORable' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic '0' when active and a high-impedance when inactive. An external pullup resistor is required.<br><br>The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not disabled. |
| 8 | ADCIN1 | I/P | Analogue to digital converter input 1 (ADC1) |
| 9 | ADCIN2 | I/P | Analogue to digital converter input 2 (ADC2) |

## 1.3 Signal List (continued)

| Package P4/D2/D5 | Signal | | Description |
|---|---|---|---|
| **Pin No.** | **Name** | **Type** | |
| 10 | ADCIN3 | I/P | Analogue to digital converter input 3 (ADC3) |
| 11 | ADCIN4 | I/P | Analogue to digital converter input 4 (ADC4) |
| 12 | $V_{SS}$ | POWER | The negative supply rail (ground) for both analogue and digital supplies. |
| 13 | $V_{BIAS}$ | O/P | An analogue bias line for the internal circuitry, held at ½ $AV_{DD}$. This pin must be decoupled by a capacitor mounted close to the device pins. |
| 14 | | N/C | No internal connection. Do not make any connection to this pin. |
| 15 | DACOUT1 | O/P | Digital to analogue converter No. 1 output (DAC1) |
| 16 | DACOUT2 | O/P | Digital to analogue converter No. 2 output (DAC2) |
| 17 | DACOUT3 | O/P | Digital to analogue converter No. 3 output (DAC3) |
| 18 | | N/C | No internal connection. Do not make any connection to this pin. |
| 19 | $AV_{DD}$ | POWER | The positive analogue supply rail. Analogue levels and voltages are dependent upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor. |
| 20 | MOD1 IN | I/P | Input to MOD1 variable attenuator. |
| 21 | MOD2 IN | I/P | Input to MOD2 variable attenuator. |
| 22 | MOD1 | O/P | Output of MOD1 variable attenuator. |
| 23 | MOD2 | O/P | Output of MOD2 variable attenuator. |
| 24 | $DV_{DD}$ | POWER | The positive digital supply rail. Digital levels and voltages are dependent upon this supply. This pin should be decoupled to $V_{SS}$ by a capacitor. |

**Notes:** I/P = Input
O/P = Output

## 1.4 External Components




| | | | | | | | |
|---|---|---|---|---|---|---|---|
| C1 | 22pF | ±20% | R1 | 1MΩ | ±5% | X1 | Note 1 |
| C2 | 22pF | ±20% | R2 | 22kΩ | ±10% | | |
| C3 | 0.1µF | ±20% | | | | | |
| C4 | 0.1µF | ±20% | | | | | |
| C5 | 0.1µF | ±20% | | | | | |

Notes: 1. If an external clock is to be used, it should be connected to Pin 2 and the components C1, C2, R1 and X1 omitted. The ADC clock frequency is derived from the crystal or external clock by means of internal programmable dividers. Refer to Section 1.7 for details of crystal or external clock frequency range.

**Figure 2: Recommended External Components**

## 1.5 General Description

The device comprises four groups of related functions: variable attenuators, digital to analogue converters, a multiplexed analogue to digital converter with multiplexer, clock generator and four 8-bit magnitude comparators with variable reference levels. These functions are all controlled by the 'C-BUS' serial interface and are described below:

**Variable Attenuators**
The two variable attenuators have a range of 0 to -12dB and 0 to -6dB respectively and may be controlled independently.

**Digital to Analogue Converters**
Three DACs are provided with default resolutions of 8 bits, which are defined at the initial chip reset. In this mode the 'C-BUS' data is transferred in a single byte. An option is provided to define any one or more of the DAC resolutions to be 10 bits, then the DAC requires the transfer of two 'C-BUS' data bytes.

The upper and lower DAC reference voltages are defined internally as $AV_{DD}$ and $V_{SS}$ respectively. The output voltage is expressed as:

$$V_{OUT} = AV_{DD} \times (DATA / 2^n) \quad [Volts]$$

Where, n is the DAC resolution (8 or 10 bits) and DATA is the decimal value of the input code. For example: n = 8 and binary code = 11111111 therefore DATA = 255

$$V_{OUT} = AV_{DD} \times (255 / 256) \quad [Volts]$$

Any one of the three DAC input latches may be loaded by sending an address/command byte followed by one or two data bytes to the 'C-BUS' interface. The data is then latched and the static voltage is updated at the appropriate output.

When a DAC is disabled its output is defined as open-circuit.

**Analogue to Digital Converter and ADC Clock Generator**
A single successive approximation ADC is provided with four multiplexed inputs. In order to minimise the sampling time of each input channel, a Sample and Hold circuit has not been included at the input of the ADC.

For the sampling to be accurate the input signal should not change significantly during the conversion time. Since the typical application is for the monitoring of slowly changing control voltages this should not present any problems. The maximum signal 'linear rate of change', 'S', can be quantified by the following expression (for a maximum 1 bit error):

$$S = AV_{DD} \times f_{adc\_clk} / (2^{10} \times 1000 \times (10 + 2)) \quad [mV/\mu s]$$

Where $f_{adc\_clk}$ is the internal ADC clock frequency.

The programmable clock generator is intended to be flexible, making use of an external system clock signal or a dedicated crystal. This clock signal is scaled to provide the internal ADC clock frequency ($f_{adc\_clk}$). The user has full control of the frequency scaling factor and this should be chosen such that the input clock frequency, at the XTAL/CLOCK pin, divided by this factor is no more than 1MHz.

The microcontroller is required to wait during the conversion time, $T_{conv\_max}$ (Figure 3), before issuing a 'READ ADC DATAx' command. If this is not done, then the converted data returned on 'C-BUS' will be the result of the previous conversion on the selected channel. It is possible for the data conversion rate to exceed the reply rate on 'C-BUS'. In such a case, the data returned will be the result of the most recent conversion completed.

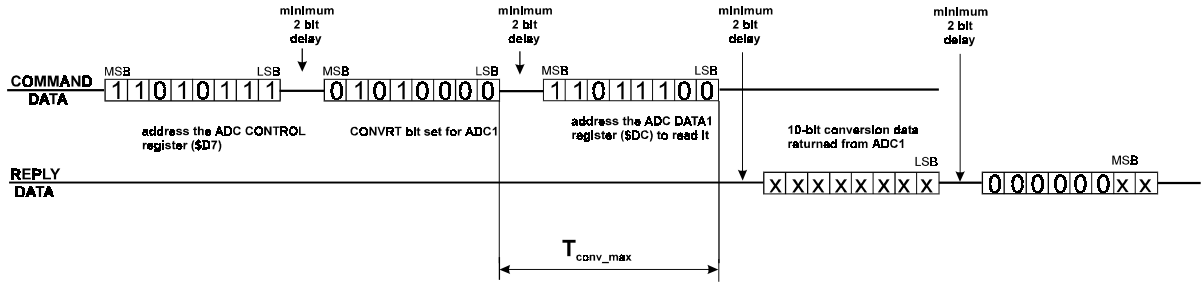



**Figure 3: Example of a "conversion and read"**

* $T_{conv\_max}$ is directly related to the ADC clock frequency, which in turn is set by the external clock frequency and the clock divider.

$$T_{conv\_max} = ((10 + 2) \times \text{'NUMBER OF ENABLED MUX INPUTS'} / f_{adc\_clk}) \quad [\text{Seconds}]$$

Note that after reading the ADC1 data, it is necessary to re-enable the conversion of data by setting Bit 5 of the ADC Control Register to '1'.

**Magnitude Comparators and Interrupt Request**

High and low digital comparator reference levels are provided for the four digital magnitude comparators via the 'C-BUS' interface. The digital input to the comparators is provided by the most significant 8 bits of each ADC data.

When the sampled data falls outside the high or low digital comparator reference levels the status register is updated and the IRQN pin is pulled low. When a reference level is set to '0', its IRQ is disabled.

### 1.5.1 Software Description

#### Address/Commands

Instructions and Data are transferred via the 'C-BUS' in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the FX839 consist of an Address/Command byte followed by either:

(i) a control or DAC data write (1 or 2 bytes) or,
(ii) a status or ADC data read (1 or 2 bytes)

### Write Only Register (8-Bit and 16-Bit)

| HEX ADDRESS/ COMMAND | REGISTER NAME | BIT 7 (D7) | BIT 6 (D6) | BIT 5 (D5) | BIT 4 (D4) | BIT 3 (D3) | BIT 2 (D2) | BIT 1 (D1) | BIT 0 (D0) |
|---|---|---|---|---|---|---|---|---|---|
| $01 | RESET | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| $D0 | CLOCK/IRQ CONTROL | 0 | 0 | 0 | 0 | 0 | DIVIDER BIT 2 | BIT 1 | BIT 0 |
| $D2 | VARIABLE ATTENUATOR (1) | 0 | 0 | MOD1 ENABLE | MOD1 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | VARIABLE ATTENUATOR (2) | 0 | 0 | MOD2 ENABLE | MOD2 BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| $D3 | DAC CONTROL | NBIT DAC1 | NBIT DAC2 | NBIT DAC3 | 0 | DAC1 ENABLE | DAC2 ENABLE | DAC3 ENABLE | 0 |
| $D4 | DAC1 DATA (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | *See Note 1 (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $D5 | DAC2 DATA (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | *See Note 1 (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $D6 | DAC3 DATA (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | *See Note 1 (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $D7 | ADC CONTROL | 0 | 1 | READN | ADCIN1 ACTIVE | ADCIN2 ACTIVE | ADCIN3 ACTIVE | ADCIN4 ACTIVE | 0 |
| $D8 | MAG COMP ONE LEVELS (1) | MAGNITUDE COMPARATOR UPPER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | MAG COMP ONE LEVELS (2) | MAGNITUDE COMPARATOR LOWER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| $D9 | MAG COMP TWO LEVELS (1) | MAGNITUDE COMPARATOR UPPER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | MAG COMP TWO LEVELS (2) | MAGNITUDE COMPARATOR LOWER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| $DA | MAG COMP THREE LEVELS (1) | MAGNITUDE COMPARATOR UPPER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | MAG COMP THREE LEVELS (2) | MAGNITUDE COMPARATOR LOWER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| $DB | MAG COMP FOUR LEVELS (1) | MAGNITUDE COMPARATOR UPPER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | MAG COMP FOUR LEVELS (2) | MAGNITUDE COMPARATOR LOWER LEVEL BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |

**Note 1:** A second byte is expected by the 'C-BUS' interface only when the 'NBIT DAC*n*' bit of the 'DAC Control Register' is set high. Otherwise the data transfer is a single byte (Bit 7 to Bit 0).

### Read Only Registers (8-Bit and 16-Bit)

| HEX ADDRESS/ COMMAND | REGISTER NAME | BIT 7 (D7) | BIT 6 (D6) | BIT 5 (D5) | BIT 4 (D4) | BIT 3 (D3) | BIT 2 (D2) | BIT 1 (D1) | BIT 0 (D0) |
|---|---|---|---|---|---|---|---|---|---|
| $D1 | IRQ FLAGS | HIRQF4 | LIRQF4 | HIRQF3 | LIRQF3 | HIRQF2 | LIRQF2 | HIRQF1 | LIRQF1 |
| $DC | ADC DATA1 (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $DD | ADC DATA2 (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $DE | ADC DATA3 (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |
| $DF | ADC DATA4 (1) | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| | (2) | 0 | 0 | 0 | 0 | 0 | 0 | BIT 9 | BIT 8 |

### Write Only Register Description

### RESET Register (Hex Address $01)

The reset command has no data attached to it. It sets the device registers into the specific states listed below:

| REGISTER NAME | BIT 7 (D7) | BIT 6 (D6) | BIT 5 (D5) | BIT 4 (D4) | BIT 3 (D3) | BIT 2 (D2) | BIT 1 (D1) | BIT 0 (D0) |
|---|---|---|---|---|---|---|---|---|
| CLOCK/IRQ CONTROL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC CONTROL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC1 DATA*1* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC2 DATA*1* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC3 DATA*1* | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ADC CONTROL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| VARIABLE ATTENUATOR (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MAG COMP ONE LEVELS (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MAG COMP TWO LEVELS (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MAG COMP THREE LEVELS (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| MAG COMP FOUR LEVELS (1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note 1:** Default resolution is defined as 8-Bits.

**CLOCK/IRQ CONTROL Register (Hex Address $D0)**
This register controls the ADC clock divide ratio:

**Bits 7 to 3** Reserved for future use. These bits should be set to '0'.

**DIVIDER (Bit 2 to Bit 0)** The input clock divide ratio, which sets the ADC clock frequency is defined in the following table:

| Bit 2 | Bit 1 | Bit 0 | Function |
|---|---|---|---|
| 0 | 0 | 0 | Powersave |
| 0 | 0 | 1 | ÷1 |
| 0 | 1 | 0 | ÷2 |
| 0 | 1 | 1 | ÷4 |
| 1 | 0 | 0 | ÷8 |
| 1 | 0 | 1 | ÷16 |
| 1 | 1 | 0 | ÷32 |
| 1 | 1 | 1 | ÷64 |

**VARIABLE ATTENUATOR Register (Hex address $D2)**

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to enable and set the attenuation of the Modulator 1 amplifier and bits 0 - 5 of the second byte in this register are used to enable and set the attenuation of the Modulator 2 amplifier, according to the tables below:

**BYTE 1**

| 5 | 4 | 3 | 2 | 1 | 0 | Mod. 1 Attenuation |
|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | Disabled ($V_{BIAS}$) |
| 1 | 0 | 0 | 0 | 0 | 0 | >40dB |
| 1 | 0 | 0 | 0 | 0 | 1 | 12.0dB |
| 1 | 0 | 0 | 0 | 1 | 0 | 11.6dB |
| 1 | 0 | 0 | 0 | 1 | 1 | 11.2dB |
| 1 | 0 | 0 | 1 | 0 | 0 | 10.8dB |
| 1 | 0 | 0 | 1 | 0 | 1 | 10.4dB |
| 1 | 0 | 0 | 1 | 1 | 0 | 10.0dB |
| 1 | 0 | 0 | 1 | 1 | 1 | 9.6dB |
| 1 | 0 | 1 | 0 | 0 | 0 | 9.2dB |
| 1 | 0 | 1 | 0 | 0 | 1 | 8.8dB |
| 1 | 0 | 1 | 0 | 1 | 0 | 8.4dB |
| 1 | 0 | 1 | 0 | 1 | 1 | 8.0dB |
| 1 | 0 | 1 | 1 | 0 | 0 | 7.6dB |
| 1 | 0 | 1 | 1 | 0 | 1 | 7.2dB |
| 1 | 0 | 1 | 1 | 1 | 0 | 6.8dB |
| 1 | 0 | 1 | 1 | 1 | 1 | 6.4dB |
| 1 | 1 | 0 | 0 | 0 | 0 | 6.0dB |
| 1 | 1 | 0 | 0 | 0 | 1 | 5.6dB |
| 1 | 1 | 0 | 0 | 1 | 0 | 5.2dB |
| 1 | 1 | 0 | 0 | 1 | 1 | 4.8dB |
| 1 | 1 | 0 | 1 | 0 | 0 | 4.4dB |
| 1 | 1 | 0 | 1 | 0 | 1 | 4.0dB |
| 1 | 1 | 0 | 1 | 1 | 0 | 3.6dB |
| 1 | 1 | 0 | 1 | 1 | 1 | 3.2dB |
| 1 | 1 | 1 | 0 | 0 | 0 | 2.8dB |
| 1 | 1 | 1 | 0 | 0 | 1 | 2.4dB |
| 1 | 1 | 1 | 0 | 1 | 0 | 2.0dB |
| 1 | 1 | 1 | 0 | 1 | 1 | 1.6dB |
| 1 | 1 | 1 | 1 | 0 | 0 | 1.2dB |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.8dB |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.4dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 0dB |

**BYTE 2**

| 5 | 4 | 3 | 2 | 1 | 0 | Mod. 2 Attenuation |
|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | Disabled ($V_{BIAS}$) |
| 1 | 0 | 0 | 0 | 0 | 0 | >40dB |
| 1 | 0 | 0 | 0 | 0 | 1 | 6.0dB |
| 1 | 0 | 0 | 0 | 1 | 0 | 5.8dB |
| 1 | 0 | 0 | 0 | 1 | 1 | 5.6dB |
| 1 | 0 | 0 | 1 | 0 | 0 | 5.4dB |
| 1 | 0 | 0 | 1 | 0 | 1 | 5.2dB |
| 1 | 0 | 0 | 1 | 1 | 0 | 5.0dB |
| 1 | 0 | 0 | 1 | 1 | 1 | 4.8dB |
| 1 | 0 | 1 | 0 | 0 | 0 | 4.6dB |
| 1 | 0 | 1 | 0 | 0 | 1 | 4.4dB |
| 1 | 0 | 1 | 0 | 1 | 0 | 4.2dB |
| 1 | 0 | 1 | 0 | 1 | 1 | 4.0dB |
| 1 | 0 | 1 | 1 | 0 | 0 | 3.8dB |
| 1 | 0 | 1 | 1 | 0 | 1 | 3.6dB |
| 1 | 0 | 1 | 1 | 1 | 0 | 3.4dB |
| 1 | 0 | 1 | 1 | 1 | 1 | 3.2dB |
| 1 | 1 | 0 | 0 | 0 | 0 | 3.0dB |
| 1 | 1 | 0 | 0 | 0 | 1 | 2.8dB |
| 1 | 1 | 0 | 0 | 1 | 0 | 2.6dB |
| 1 | 1 | 0 | 0 | 1 | 1 | 2.4dB |
| 1 | 1 | 0 | 1 | 0 | 0 | 2.2dB |
| 1 | 1 | 0 | 1 | 0 | 1 | 2.0dB |
| 1 | 1 | 0 | 1 | 1 | 0 | 1.8dB |
| 1 | 1 | 0 | 1 | 1 | 1 | 1.6dB |
| 1 | 1 | 1 | 0 | 0 | 0 | 1.4dB |
| 1 | 1 | 1 | 0 | 0 | 1 | 1.2dB |
| 1 | 1 | 1 | 0 | 1 | 0 | 1.0dB |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.8dB |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.6dB |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.4dB |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.2dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 0dB |

X = don't care

**MOD1 ENABLE (Bit 5, first byte)** When this bit is '1' the MOD1 attenuator is enabled. When this bit is '0' the MOD1 attenuator is disabled (i.e. powersaved).

**MOD2 ENABLE (Bit 5, second byte)** When this bit is '1' the MOD2 attenuator is enabled. When this bit is '0' the MOD2 attenuator is disabled (i.e. powersaved).

**(Bits 7 and 6, first and second bytes)** Reserved for future use. These should be set to '0'.

**DAC CONTROL Register (Hex address $D3)**
This register controls the resolution and the number of enabled DAC outputs:

**NBIT DAC1, NBIT DAC2, NBIT DAC3**
**(Bit 7 to Bit 5)** These bits define the input resolutions for each of the four DACs. When 'NBIT DAC*n*' is '0' the resolution of DAC*n* is 8-Bits. When 'NBIT DAC*n* is '1' the resolution of DAC*n* is 10-Bits.

**Bit 4** Reserved for future use. This bit should be set to '0'.

**DAC1 ENABLE, DAC2 ENABLE, DAC3 ENABLE**
**(Bit 3 to Bit 1)** These bits allow any one or more of the three DACs to be powered up. When '0' the DAC*n* is powered down and the output is high impedance. When '1' the DAC is powered on and the output voltage is defined by the DAC Data Registers.

**Bit 0** Reserved for future use. This bit should be set to '0'.

**DAC1 DATA Register (Hex Address $D4)**
**DAC2 DATA Register (Hex Address $D5)**
**DAC3 DATA Register (Hex Address $D6)**

The data in these three registers sets the analogue voltage at the output of DAC1, DAC2 and DAC3. This data will consist of one or two bytes depending on the defined input resolution which is set by bits 7, 6 and 5 of the DAC Control Register. When operating with 10-bit resolution Bit 7 to Bit 2 of the DAC*n* DATA Register second data byte must be set to "0".

**ADC CONTROL Register (Hex Address $D7)**
This register controls the resolution, active inputs and conversion modes of the ADC as described below:

**Bit 7** Reserved for future use. This bit should be set to '0'.

**Bit 6** Reserved for future use. This bit should be set to '1'.
(On reset, this bit is set to '0').

**READN (Bit 5)** When this bit is set to '1' all active input channels are continuously sampled and the latest converted data stored for each channel. When this bit is set to '0' all conversions are stopped so that they may be read.

**ADC1 ACTIVE, ADC2 ACTIVE, ADC3 ACTIVE, ADC4 ACTIVE**
**(Bit 4 to Bit 1)** These bits allow any one or more of the four ADC input channels to be enabled. When '0' the ADCIN*n* input voltage is not converted. When '1' the ADCIN*n* input is defined as active and the input voltage is converted.

Note: ADC1 must always be enabled for any other channel to work.

**(Bit 0)** Reserved for future use. This bit should be set to '0'.

**MAG COMP ONE LEVELS (Hex Address $D8)**
**MAG COMP TWO LEVELS (Hex Address $D9)**
**MAG COMP THREE LEVELS (Hex Address $DA)**
**MAG COMP FOUR LEVELS (Hex Address $DB)**

Each address controls the relevant numbered ADC magnitude comparator.

The first byte, transmitted with the most significant bit first, sets the magnitude comparator upper reference level and the second byte sets the magnitude comparator lower reference level.

When a reference level's value is set to '0' its IRQ is disabled.

If a reference level's value is set to 'FF', the level will correspond to:

$$V_{REF} = AV_{DD} \times (255 / 256) \quad [Volts]$$

**Read Only Register Description**

**IRQ FLAGS Register (Hex Address $D1)**

**HIRQF1, HIRQF2, HIRQF3, HIRQF4**
**(Bit 1) (Bit 3) (Bit 5) (Bit 7)**

These bits are set if the relevant digital magnitude comparator input exceeds its upper reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.

**LIRQF1, LIRQF2, LIRQF3, LIRQF4**
**(Bit 0) (Bit 2) (Bit 4) (Bit 6)**

These bits are set if the relevant digital magnitude comparator input falls below its lower reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.

**ADC DATA1 Register (Hex Address $DC)**
**ADC DATA2 Register (Hex Address $DD)**
**ADC DATA3 Register (Hex Address $DE)**
**ADC DATA4 Register (Hex Address $DF)**

This data will consist of two bytes each. Bit 7 to Bit 2 of the second data byte will be set to '0'.

## 1.6 Application Notes

### 1.6.1 General

1.6.1.1 ‘C-BUS’ Clock
Although this is specified as a 500kHz clock for compatibility with other ‘C-BUS’ devices, the FX839 ‘C-BUS’ will operate over a much wider range. Users should ensure that the ‘C-BUS’ clock is at least 4 times slower than the crystal or external clock on Pin 2 of the FX839.

## 1.7 Performance Specification

### 1.7.1 Electrical Performance

**Absolute Maximum Ratings**
Exceeding these maximum ratings can result in damage to the device.

| | Min. | Max. | Units |
|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) (either $AV_{DD}$ or $DV_{DD}$) | -0.3 | 7.0 | V |
| Voltage on any pin to $V_{SS}$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Current into or out of $AV_{DD}$, $DV_{DD}$ and $V_{SS}$ pins | -30 | +30 | mA |
| Current into or out of any other pin | -20 | +20 | mA |
| $AV_{DD}$ - $DV_{DD}$ | -100 | +100 | mV |

| **P4/D2 Package** | **Min.** | **Max.** | **Units** |
|---|---|---|---|
| Total Allowable Power Dissipation at Tamb = 25°C | | 800 | mW |
| ... Derating | | 13 | mW/°C |
| Storage Temperature | -55 | +125 | °C |
| Operating Temperature | -40 | +85 | °C |

| **D5 Package** | **Min.** | **Max.** | **Units** |
|---|---|---|---|
| Total Allowable Power Dissipation at Tamb = 25°C | | 550 | mW |
| ... Derating | | 9 | mW/°C |
| Storage Temperature | -55 | +125 | °C |
| Operating Temperature | -40 | +85 | °C |

**Operating Limits**
Correct operation of the device outside these limits is not implied.

| | **Notes** | **Min.** | **Max.** | **Units** |
|---|---|---|---|---|
| Supply ($V_{DD}$ - $V_{SS}$) (either $AV_{DD}$ or $DV_{DD}$) | | 3.0 | 5.5 | V |
| Operating Temperature | | -40 | +85 | °C |
| Xtal Frequency | | 0.5 | 6.0 | MHz |

**Operating Characteristics**

For the following conditions unless otherwise specified:
$AV_{DD} = DV_{DD} = V_{DD}$ = 3.3V to 5.0V, Tamb = - 40°C to +85°C.

| | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **DC Parameters** | | | | | |
| Supply Voltage ($DV_{DD}$) | | 3.0 | 5.0 | 5.5 | V |
| Supply Voltage ($AV_{DD}$) | | 3.0 | 5.0 | 5.5 | V |
| Supply Difference ($AV_{DD}$ - $DV_{DD}$) | | -100 | - | 100 | mV |
| $I_{DD}$ (powersaved) $V_{DD}$ = 5V | | - | 250 | 400 | µA |
| $I_{DD}$ (not powersaved) $V_{DD}$ = 5V | | - | 4.5 | 7.0 | mA |
| $I_{DD}$ (powersaved) $V_{DD}$ = 3.3V | | - | 150 | 250 | µA |
| $I_{DD}$ (not powersaved) $V_{DD}$ = 3.3V | | - | 2.5 | 4.0 | mA |
| **'C-BUS' Interface** | | | | | |
| Input Logic '1' | | 70% | | | $DV_{DD}$ |
| Input Logic '0' | | | | 30% | $DV_{DD}$ |
| Input Leakage Current (Logic '1' and '0') | | -1.0 | | 1.0 | µA |
| Input Capacitance | | | | 7.5 | pF |
| Output Logic '1' ($I_{OH}$ = 120µA) | | 90% | | | $DV_{DD}$ |
| Output Logic '0' ($I_{OL}$ = 360µA) | | | | 10% | $DV_{DD}$ |
| **DACs and Output Buffers (Guaranteed monotonic)** | | | | | |
| **(a) Un-loaded Performance** | | | | | |
| Resolution | | | 8 or 10 | | Bits |
| Internal DAC Settling Time (to 0.5 lsb) | | | | 10.0 | µs |
| Integral non-linearity (8-Bit mode) | 6 | | | 3.0 | LSBs |
| Integral non-linearity (10-Bit mode) | 6 | | | 5.0 | LSBs |
| Differential non-linearity (8-Bit mode) | 5 | | | 1.0 | LSBs |
| Differential non-linearity (10-Bit mode) | 5 | | | 1.0 | LSBs |
| Buffer Slew Rate (with 20pF load) | | | | TBD | V/µs |
| Buffer Output Resistance (open loop) | | | | 200 | Ω |
| Zero Error | | -20 | 0 | 20 | mV |
| RMS Output Noise Voltage (Low Pass Filter of 30kHz bandwidth) | | | 10 | | µV |
| **(b) Loaded Performance** | 1 | | | | |
| Output voltage with resistive load to ground (Digital code = $3FF_{HEX}$) | | 4.79 | | | V |
| Output voltage with resistive load to ground (Digital code = $200_{HEX}$, 10 Bit) or (Digital code = $80_{HEX}$, 8 Bit) | 3 | | 2.495 | | V |
| Output voltage with resistive load to $V_{DD}$ (Digital code = $000_{HEX}$) | 3 | | | 200 | mV |
| Minimum Resistive Load | | 1.0 | | | kΩ |

| | | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ADCs and Multiplexed Inputs (Guaranteed monotonic)** | | | | | | |
| Resolution | | | | 10 | | Bits |
| Input signal 'linear rate of change' $V_{DD}$ = 3.3V, $f_{adc\_clk}$ = (For 1 Bit error) | | | | | 0.27 | mV/µs |
| Conversion Time $f_{adc\_clk}$ = 1MHz | | | | 12 | | µs |
| Integral non-linearity | | | | | 2.0 | LSBs |
| Differential non-linearity | | | | | 1.0 | LSBs |
| Zero error | | | -20 | | 20 | mV |
| ADC Clock Frequency ($f_{adc\_clk}$) | | | | 1.0 | TBD | MHz |
| Input Capacitance | | | | TBD | | pF |
| **Variable Attenuators** | | | | | | |
| Nominal Adjustment Range | (MOD1) | | 0 | | 12.0 | dB |
| | (MOD2) | | 0 | | 6.0 | dB |
| Attenuation Accuracy | | | -1.0 | | 1.0 | dB |
| Step Size | (MOD1) | | 0.2 | 0.4 | 0.6 | dB |
| | (MOD2) | | 0.1 | 0.2 | 0.3 | dB |
| Output Impedance | | 2 | | 600 | | Ω |
| Bandwidth (-3dB) | | 2 | | 100 | | kHz |
| Input Impedance (at 100Hz) | | | | 15.0 | | kΩ |
| **Magnitude Comparators and Interrupt Request** | | | | | | |
| Resolution | | | | 8 | | Bits |
| Output Logic '0' at IRQN ($I_{OL}$= 360µA and R2 = 22kΩ ± 10% to $DV_{DD}$) | | | | | 10% | $DV_{DD}$ |
| 'Off' State Leakage Current at IRQN (Vout = $DV_{DD}$) | | | | | 10 | µA |
| **Xtal/Clock Input** | | | | | | |
| Frequency Range | | 4 | 0.5 | | 6.0 | MHz |
| 'High' pulse width | | | 40 | | | ns |
| 'Low' pulse width | | | 40 | | | ns |
| Input Impedance (at 100Hz) | | | | 10 | | MΩ |
| Gain (I/P = 1mVrms at 100Hz) | | | | 20 | | dB |

Notes: 1. The extremes of the DAC output range, when resistively loaded, are affected by the output impedance of the DAC buffer. Under these conditions the output impedance can approach 200Ω. However, when the output is operating well within the supply, the closed loop output impedance will be significantly lower thereby improving the loaded performance.

2. Small signal impedance, at $AV_{DD}$ = 5V and Tamb = 25°C.

Notes: 3. $R_{LOAD}$ = 5kΩ $AV_{DD}$ = 5.0V.

4. At $V_{DD}$ = 5.0V only. The 'C-BUS' clock must be at least 4 times slower than this xtal/clock frequency.

5. Differential non-linearity is defined as the difference in width between adjacent code midpoints and the width of an ideal LSB, divided by the width of an ideal LSB.

6. Integral non-linearity is defined as the width difference between an actual code midpoint and the line of best fit through all code midpoints, divided by the width of an ideal LSB.

### 1.7.1 **Electrical Performance** (continued)

**Timing Diagrams**

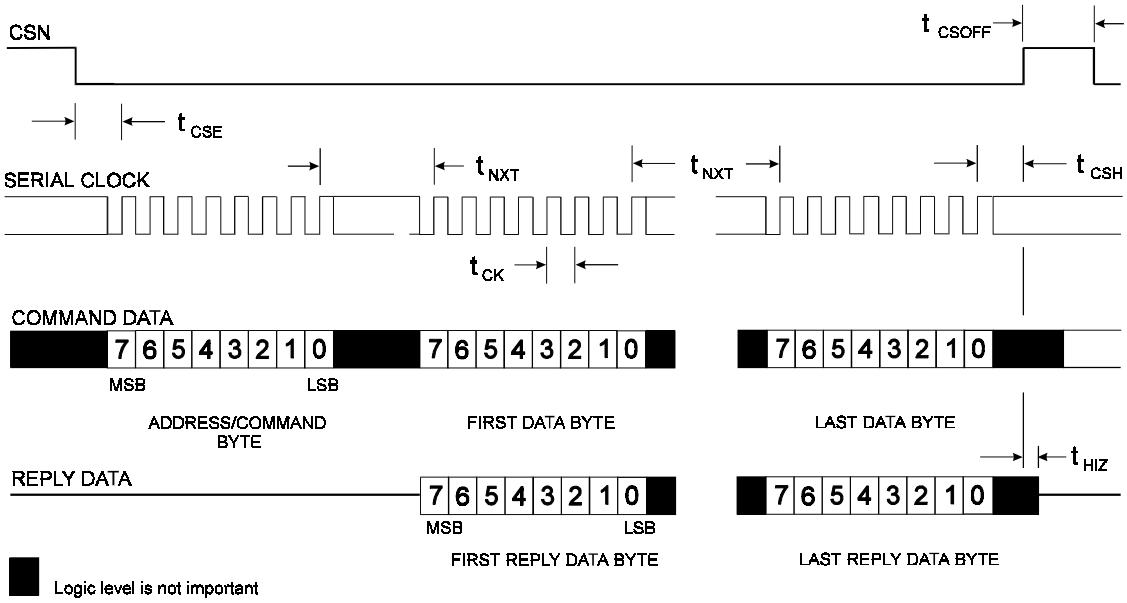



**Figure 4: 'C-BUS' Timing**

For the following conditions unless otherwise specified:

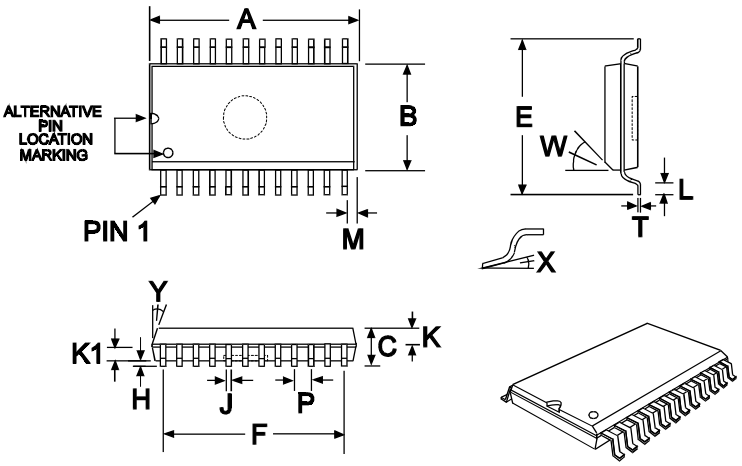
$DV_{DD}$ = 3.3V to 5.0V, Tamb = -40°C to +85°C.

| | Parameter | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CSE}$ | "CS-Enable to Clock-High" | | 2.0 | | - | µs |
| $t_{CSH}$ | Last "Clock-High to CS-High" | | 4.0 | | - | µs |
| $t_{HIZ}$ | "CS-High to Reply Output 3-state" | | - | | 2.0 | µs |
| $t_{CSOFF}$ | "CS-High" Time between transactions | | 2.0 | | - | µs |
| $t_{NXT}$ | "Inter-Byte" Time | | 4.0 | | - | µs |
| $t_{CK}$ | "Clock-Cycle" time | | 2.0 | | - | µs |

**Notes:**

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats 'C-BUS' compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

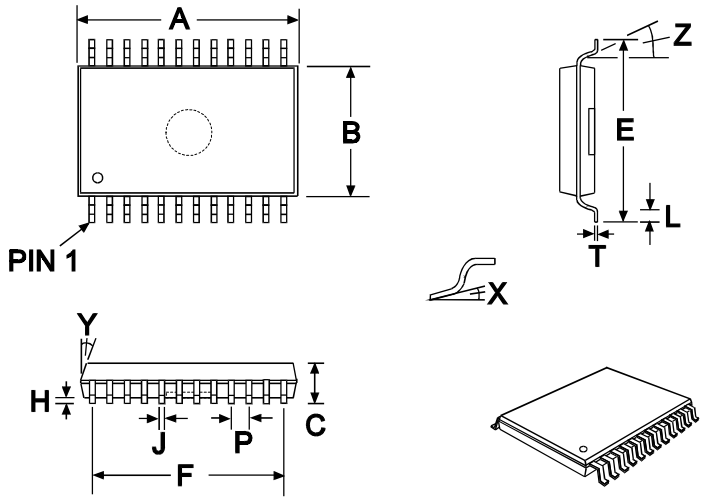
### 1.7.2 Packaging




| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.597 (15.16) | | 0.613 (15.57) |
| B | 0.291 (7.39) | | 0.299 (7.59) |
| C | 0.093 (2.36) | | 0.105 (2.67) |
| E | 0.394 (10.01) | | 0.419 (10.64) |
| F | | 0.566 (14.37) | |
| H | 0.004 (0.10) | | 0.012 (0.30) |
| J | 0.014 (0.36) | | 0.018 (0.46) |
| K | 0.036 (0.91) | | 0.046 (1.17) |
| K1 | 0.036 (0.91) | | 0.046 (1.17) |
| L | 0.016 (0.41) | | 0.050 (1.27) |
| M | 0.021 (0.53) | | 0.031 (0.79) |
| P | | 0.050 (1.27) | |
| T | 0.009 (0.23) | | 0.012 (0.30) |
| W | | 45° | |
| X | 0° | | 8° |
| Y | | 7° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**Figure 5: D2 Mechanical Outline: *Order as part no. FX839D2***

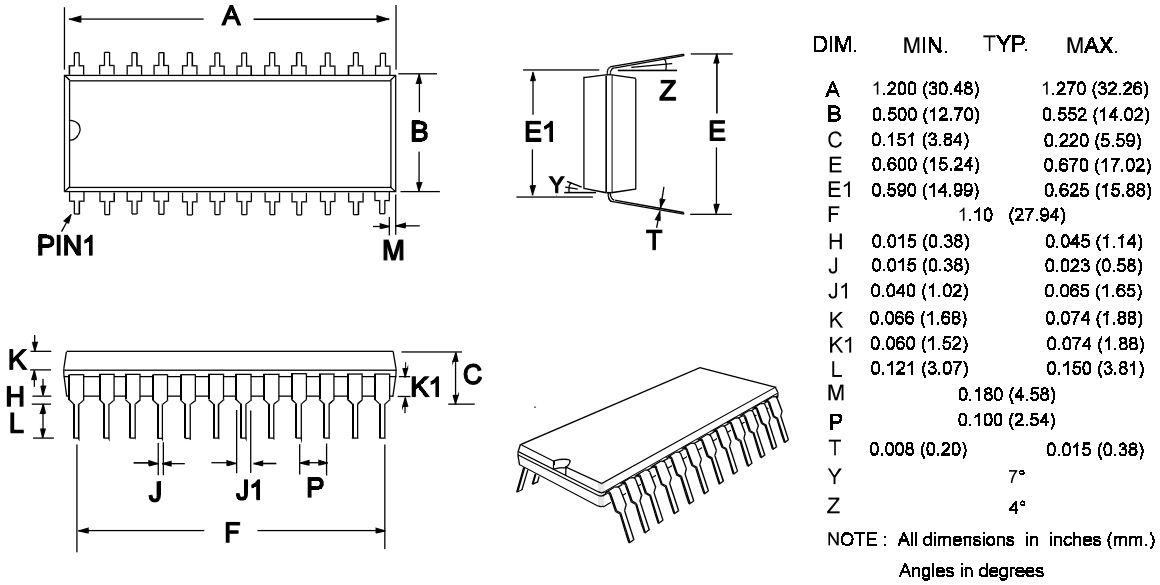



| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 0.318 (8.07) | | 0.328 (8.33) |
| B | 0.205 (5.20) | | 0.212 (5.38) |
| C | 0.068 (1.73) | | 0.078 (1.99) |
| E | 0.301 (7.65) | | 0.311 (7.90) |
| F | | 0.286 (7.15) | |
| H | 0.002 (0.05) | | 0.008 (0.21) |
| J | 0.010 (0.25) | | 0.015 (0.38) |
| L | 0.022 (0.55) | | 0.037 (0.95) |
| P | | 0.026 (0.65) | |
| T | 0.005 (0.13) | | 0.009 (0.22) |
| X | 0° | | 8° |
| Y | 7° | | 9° |
| Z | 4° | | 10° |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**Figure 6: D5 Mechanical Outline: *Order as part no. FX839D5***

### 1.7.2 Packaging




| DIM. | MIN. | TYP. | MAX. |
|---|---|---|---|
| A | 1.200 (30.48) | | 1.270 (32.26) |
| B | 0.500 (12.70) | | 0.552 (14.02) |
| C | 0.151 (3.84) | | 0.220 (5.59) |
| E | 0.600 (15.24) | | 0.670 (17.02) |
| E1 | 0.590 (14.99) | | 0.625 (15.88) |
| F | | 1.10 (27.94) | |
| H | 0.015 (0.38) | | 0.045 (1.14) |
| J | 0.015 (0.38) | | 0.023 (0.58) |
| J1 | 0.040 (1.02) | | 0.065 (1.65) |
| K | 0.066 (1.68) | | 0.074 (1.88) |
| K1 | 0.060 (1.52) | | 0.074 (1.88) |
| L | 0.121 (3.07) | | 0.150 (3.81) |
| M | | 0.180 (4.58) | |
| P | | 0.100 (2.54) | |
| T | 0.008 (0.20) | | 0.015 (0.38) |
| Y | | 7° | |
| Z | | 4° | |

NOTE : All dimensions in inches (mm.)
Angles in degrees

**Figure 7: P4 Mechanical Outline:** ***Order as part no. FX839P4***



**CONSUMER MICROCIRCUITS LIMITED**

**1 WHEATON ROAD**
**WITHAM - ESSEX**
**CM8 3TD - ENGLAND**

**Telephone: +44 1376 513833**
**Telefax: +44 1376 518247**
**e-mail: sales@cmlmicro.co.uk**
**http://www.cmlmicro.co.uk**