MRF172

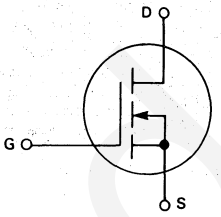
The RF MOSFET Line

2

N-CHANNEL ENHANCEMENT-MODE
RF POWER FIELD-EFFECT TRANSISTOR

. . . designed primarily for wideband large-signal output and driver stages in the 2.0–200 MHz frequency range.

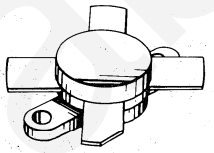
- Guaranteed Performance at 150 MHz, 28 Vdc
  Output Power = 80 Watts
  Minimum Gain = 10 dB
  Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure— 1.5 dB Typ at 2.0 A, 150 MHz

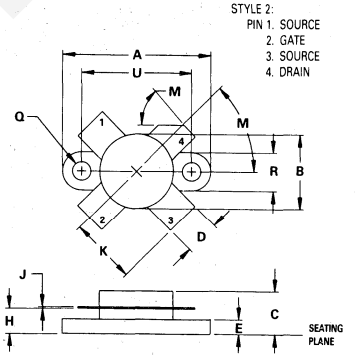


Island Labs

80 W 2.0-200 MHz

N-CHANNEL MOS
BROADBAND RF POWER
FET





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.39	25.14	0.960	0.990
B	11.82	12.95	0.465	0.510
C	5.82	6.98	0.229	0.275
D	5.49	5.96	0.216	0.235
E	2.14	2.79	0.084	0.110
H	3.66	4.52	0.144	0.178
J	0.08	0.17	0.003	0.007
K	11.05	—	0.435	—
M	45° NOM		45° NOM	
Q	2.93	3.30	0.115	0.130
R	6.25	6.47	0.246	0.255
U	18.29	18.54	0.720	0.730

CASE 211-11

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain — Source Voltage	V_{DSS}	65	Vdc
Drain — Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate — Source Voltage	V_{GS}	±40	Vdc
Drain Current — Continuous	I_D	9.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	220 1.26	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

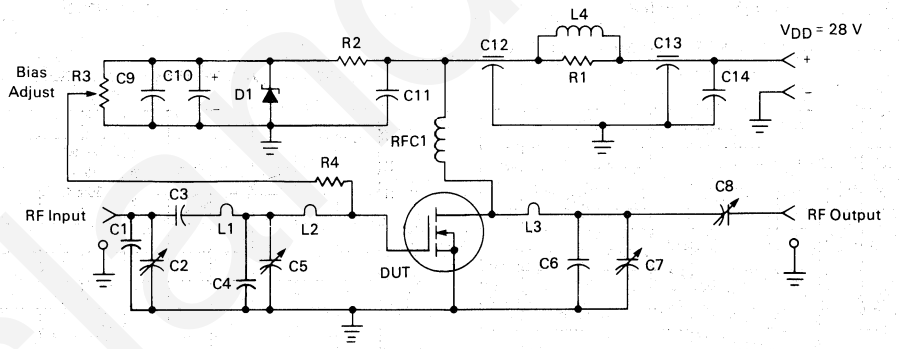
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.80	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	5.0	mAdc
Gate-Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 50 mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.0 A)	g_{fs}	1.2	1.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	100	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	135	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	26	—	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V_{DD} = 28 Vdc, I_D = 2.0 A, f = 150 MHz)	NF	—	1.5	—	dB
Common Source Power Gain (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	G_{ps}	10	12.3	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA)	η	50	60	—	%
Electrical Ruggedness (V_{DD} = 28 Vdc, P_{out} = 80 W, f = 150 MHz, I_{DQ} = 50 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

FIGURE 1 — 150 MHz TEST CIRCUIT



C1 — 25 pF Unleco
C2, C5, C7 — Arco 462, 5-80 pF
C3 — 100 pF Unleco
C4 — 40 pF Unleco
C6 — 60 pF Unleco
C8 — Arco 463, 9-180 pF
C9, C11, C14 — 0.1 μF Erie Redcap
C10 — 50 μF, 50 V
C12, C13 — 680 pF Feedthru
D1 — 1N5925A Motorola Zener

L1 — #16 AWG, 1-1/4 Turns, 0.213" ID
L2 — #16 AWG, Hairpin 0.25" × 0.062"
L3 — #14 AWG, Hairpin 0.47" × 0.2"
L4 — 10 Turns #16 AWG Enameled Wire on R1
RFC1 — 18 Turns #16 AWG Enameled Wire, 0.3" ID
R1 — 10 Ω, 2.0 W
R2 — 1.8 kΩ, 1/2 W
R3 — 10 kΩ, 10 Turn Bourns
R4 — 10 kΩ, 1/4 W

FIGURE 2 — OUTPUT POWER versus INPUT POWER

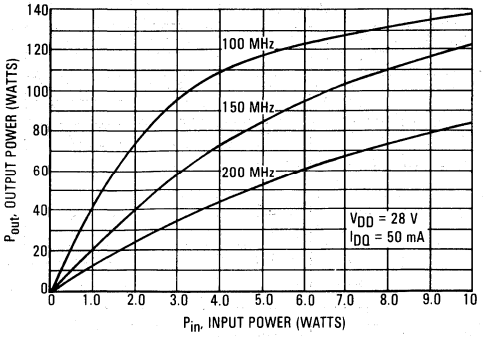


FIGURE 3 — OUTPUT POWER versus INPUT POWER

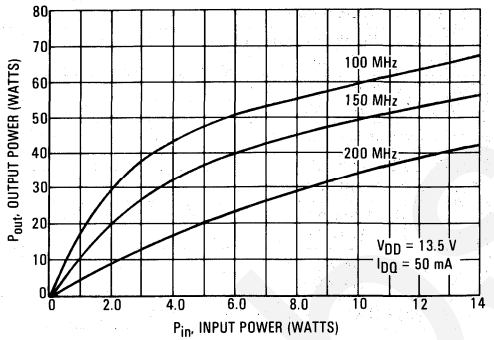


FIGURE 4 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 100 MHz

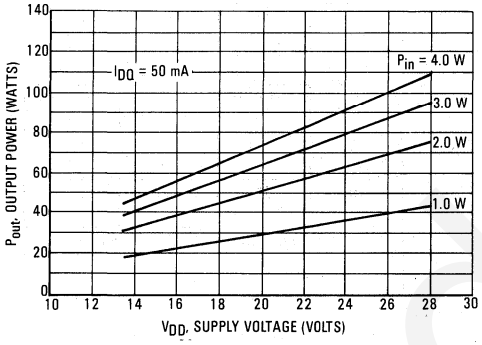


FIGURE 5 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 150 MHz

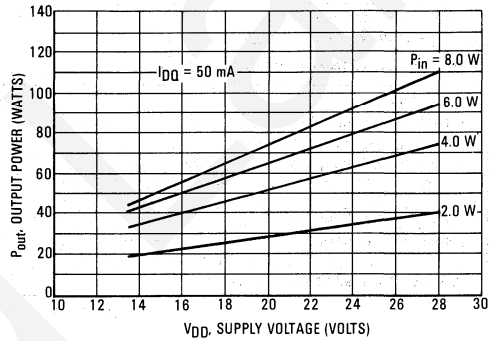


FIGURE 6 — OUTPUT POWER versus SUPPLY VOLTAGE
f = 200 MHz

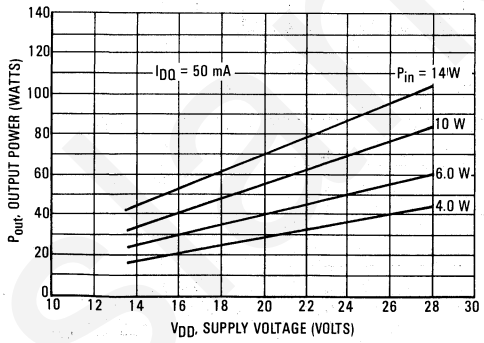


FIGURE 7 — POWER GAIN versus FREQUENCY

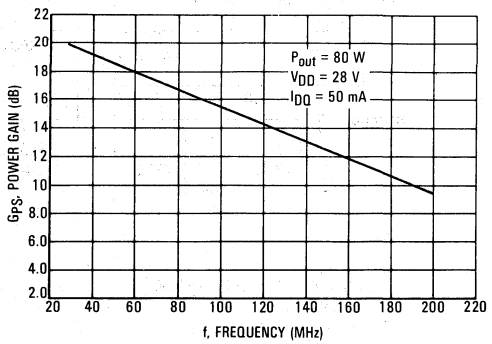


FIGURE 8 — OUTPUT POWER versus GATE VOLTAGE

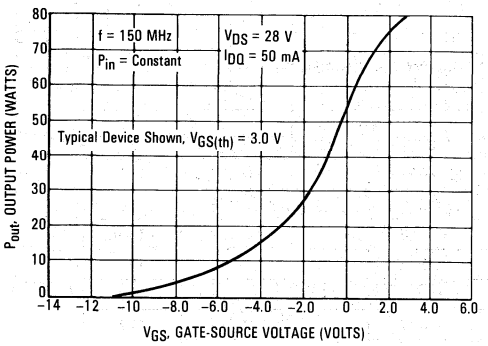


FIGURE 9 — DRAIN CURRENT versus GATE VOLTAGE (TRANSFER CHARACTERISTICS)

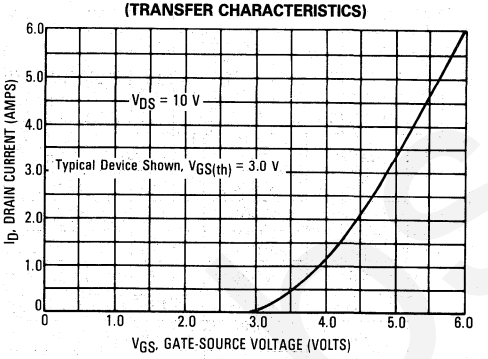


FIGURE 10 — GATE-SOURCE VOLTAGE versus CASE TEMPERATURE

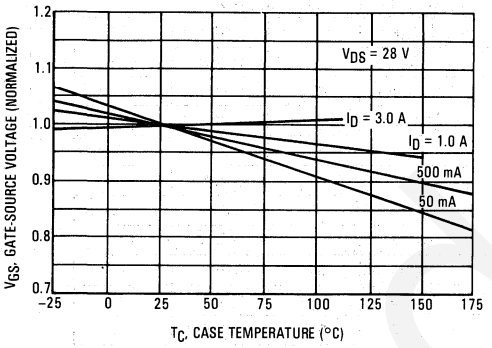


FIGURE 11 — CAPACITANCE versus DRAIN VOLTAGE

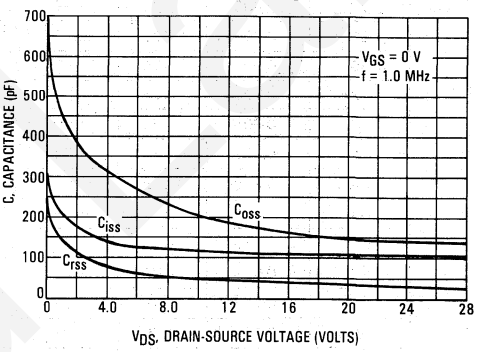


FIGURE 12 — DC SAFE OPERATING AREA

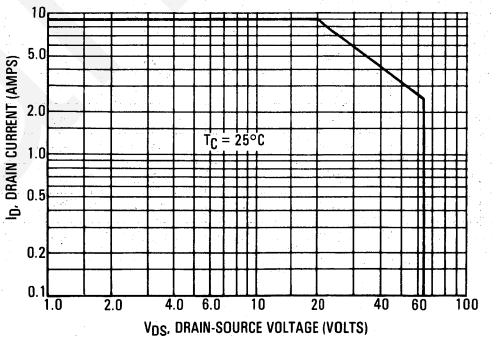


FIGURE 13 — COMMON SOURCE SCATTERING PARAMETERS
V_{DS} = 28 V, I_D = 2.0 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
2.0	0.928	–112	87.5	122	0.013	34	0.776	–128
5.0	0.902	–149	40.5	104	0.015	17	0.857	–158
10	0.897	–164	20.7	96	0.016	12	0.872	–169
20	0.896	–172	10.4	90	0.016	13	0.876	–174
30	0.896	–175	6.94	88	0.016	17	0.877	–176
40	0.896	–176	5.20	85	0.017	21	0.878	–177
50	0.897	–177	4.15	83	0.017	25	0.879	–177
60	0.897	–177	3.45	82	0.017	29	0.880	–177
70	0.898	–178	2.95	80	0.018	33	0.881	–177
80	0.899	–178	2.57	78	0.019	37	0.882	–177
90	0.901	–178	2.27	76	0.020	40	0.883	–177
100	0.903	–178	2.00	74	0.021	42	0.885	–177
110	0.905	–178	1.80	73	0.022	44	0.887	–177
120	0.907	–178	1.62	71	0.024	45	0.888	–177
130	0.908	–178	1.51	70	0.026	47	0.895	–177
140	0.909	–178	1.39	70	0.027	49	0.895	–177
150	0.910	–178	1.30	69	0.028	51	0.895	–177
160	0.911	–178	1.22	68	0.029	51	0.897	–177
170	0.912	–179	1.14	66	0.030	52	0.899	–177
180	0.921	–179	1.08	65	0.032	54	0.900	–177
190	0.921	–179	1.01	64	0.033	55	0.903	–177
200	0.922	–179	0.974	63	0.035	56	0.905	–177
210	0.920	–179	0.928	61	0.036	58	0.907	–176
220	0.915	–179	0.872	60	0.038	59	0.907	–176
230	0.915	–179	0.828	60	0.040	60	0.914	–176
240	0.917	–179	0.793	59	0.042	61	0.917	–176
250	0.922	–179	0.772	59	0.044	62	0.918	–176
260	0.927	+179	0.744	57	0.046	62	0.920	–176
270	0.928	+179	0.714	57	0.048	63	0.920	–176
280	0.929	+179	0.689	56	0.049	64	0.923	–176
290	0.929	+179	0.662	55	0.051	65	0.923	–176
300	0.938	+179	0.642	55	0.053	65	0.923	–176

FIGURE 14 — S_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

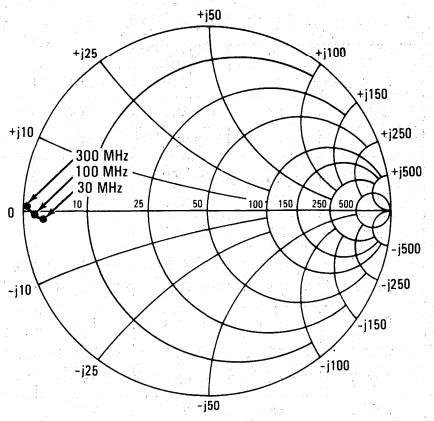


FIGURE 15 — S_{12}, REVERSE TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

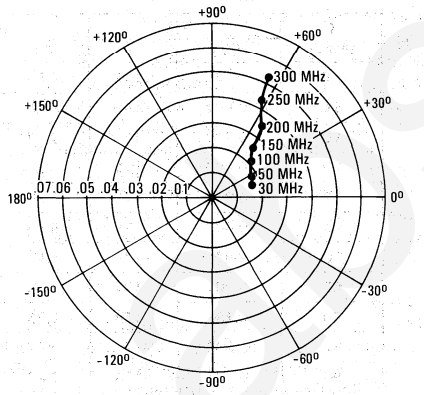


FIGURE 16 — S_{21}, FORWARD TRANSMISSION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A

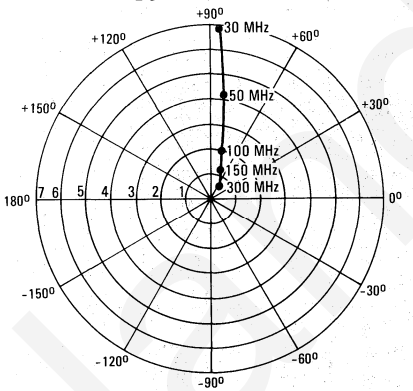
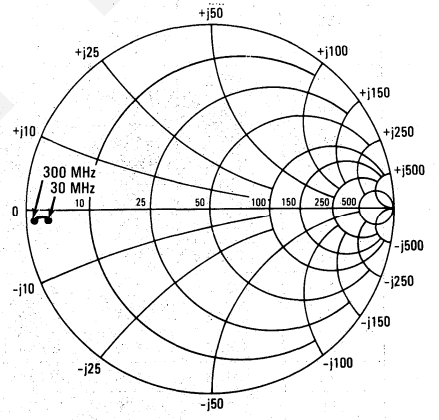


FIGURE 17 — S_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY
V_{DS} = 28 V I_D = 2.0 A



DESIGN CONSIDERATIONS

The MRF172 is a RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN-211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF172 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF161 was characterized at I_{DQ} = 50 mA, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF172 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for the MRF172. See Motorola Application Note AN-721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FET's helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

FIGURE 18 — 150 MHz TEST CIRCUIT

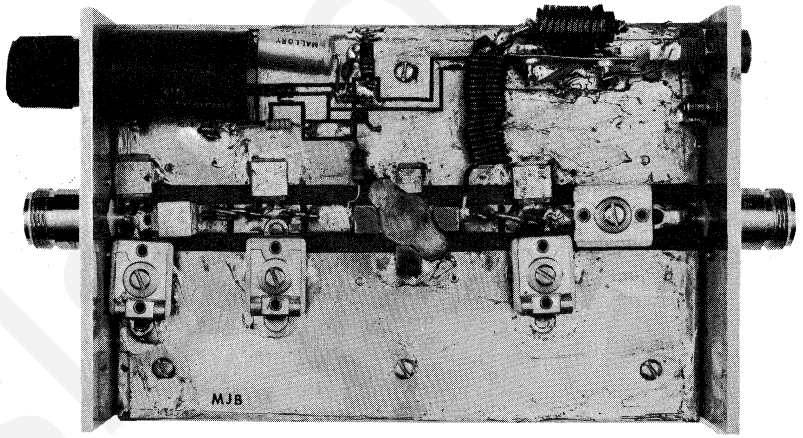
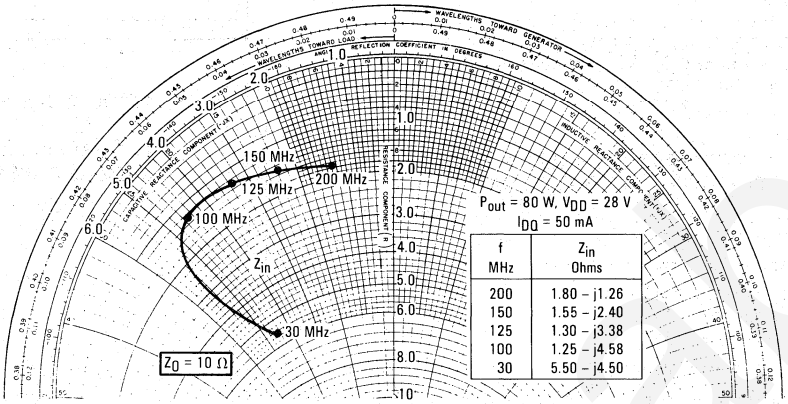
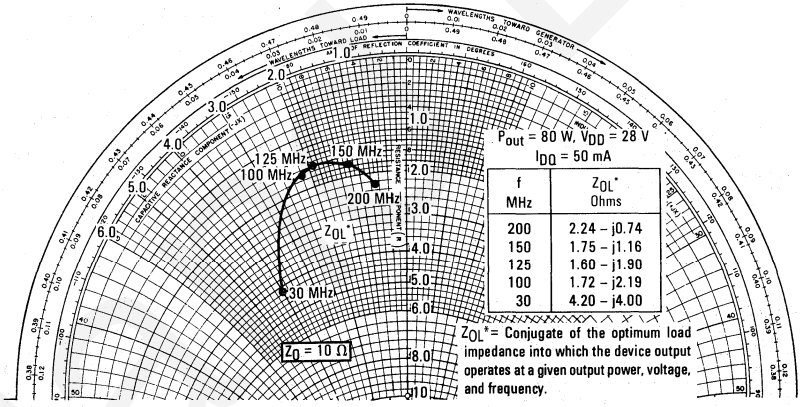


FIGURE 19 — SERIES EQUIVALENT INPUT IMPEDANCE, Z_{in}



f MHz	Z_{in} Ohms
200	1.80 – j1.26
150	1.55 – j2.40
125	1.30 – j3.38
100	1.25 – j4.58
30	5.50 – j4.50

FIGURE 20 — SERIES EQUIVALENT OUTPUT IMPEDANCE, Z_{OL}^*



f MHz	Z_{OL}^* Ohms
200	2.24 – j0.74
150	1.75 – j1.16
125	1.60 – j1.90
100	1.72 – j2.19
30	4.20 – j4.00

Z_{OL}^* = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage, and frequency.